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Project Code & Schematics Subject: M612 PVT Main Board

PCB P/N: 黃田
翰宇博德

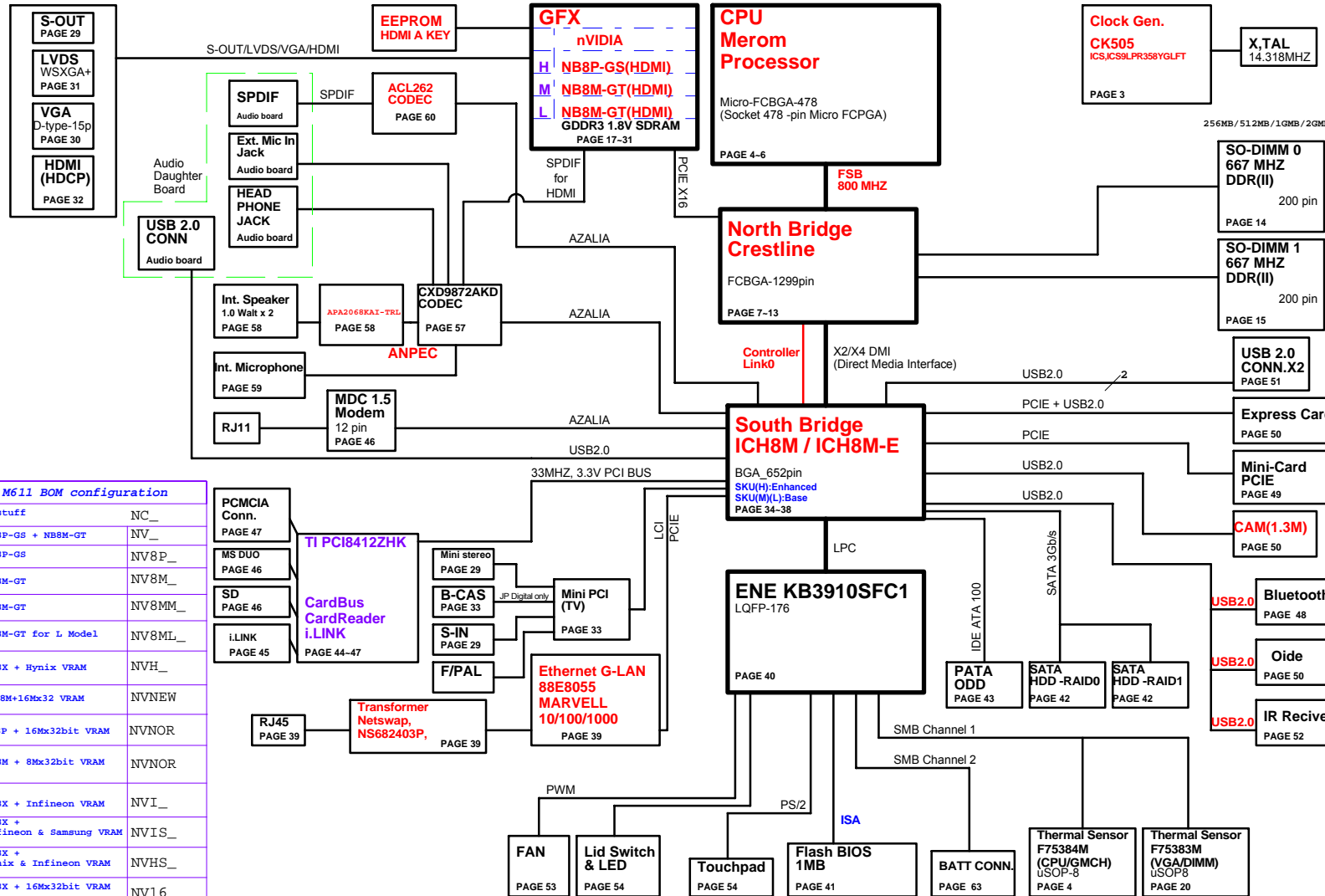
P. Leader	Check by	Design by

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
Index Page			
Size	Document Number	Rev	
A3	M612 PVT Main Board (15X176) 2007.8.24	1.0	
Date	Friday, August 31, 2007	Sheet	5 of 8



M612(Beagle Santa Rosa)Block Diagram

Red texts:
New modified



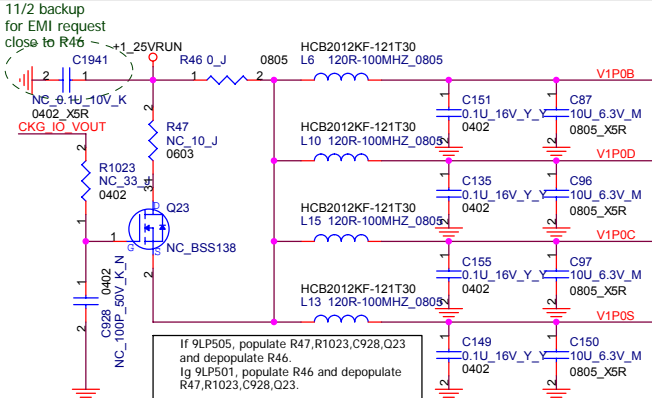
M611 BOM configuration

unstuff	NC_
NB8P-GS + NB8M-GT	NV_
NB8P-GS	NV8P_
NB8M-GT	NV8M_
NB8M-GT	NV8MM_
NB8M-GT for L Model	NV8ML_
NB8X + Hynix VRAM	NVH_
NB8M+16Mx32 VRAM	NVNEW
NB8P + 16Mx32bit VRAM	NVNOR
NB8M + 8Mx32bit VRAM	NVNOR
NB8X + Infineon VRAM	NVI_
NB8X + Infineon + Samsung VRAM	NVIS_
NB8X + Hynix + Infineon VRAM	NVHS_
NB8X + 16Mx32bit VRAM	NV16_
NB8X + 8Mx32bit VRAM	NV8_

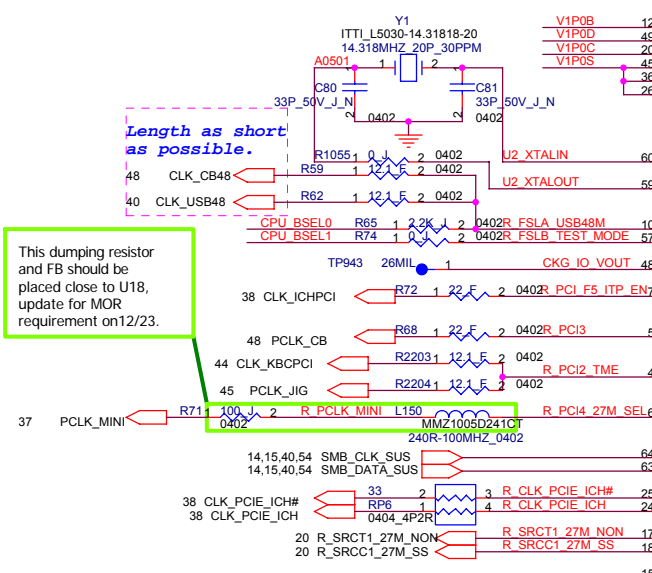
*JP Digital TV Tuner SKU unstuff JDTVNC_

Mini PCI CONN, BT CONN, IR CONN, Felica CONN unstuff for L Model LNC_

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
Block Diagram			
Size	Document Number	Rev	
C	(M612-1-01 MainBoard (MBX-176) 2007.8.24	1.0	



If 9LP505, populate R47, R1023, C928, Q23 and depopulate R46.
If 9LP501, populate R46 and depopulate R47, R1023, C928, Q23.

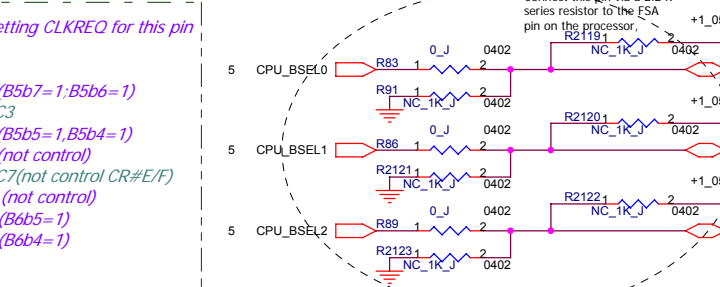
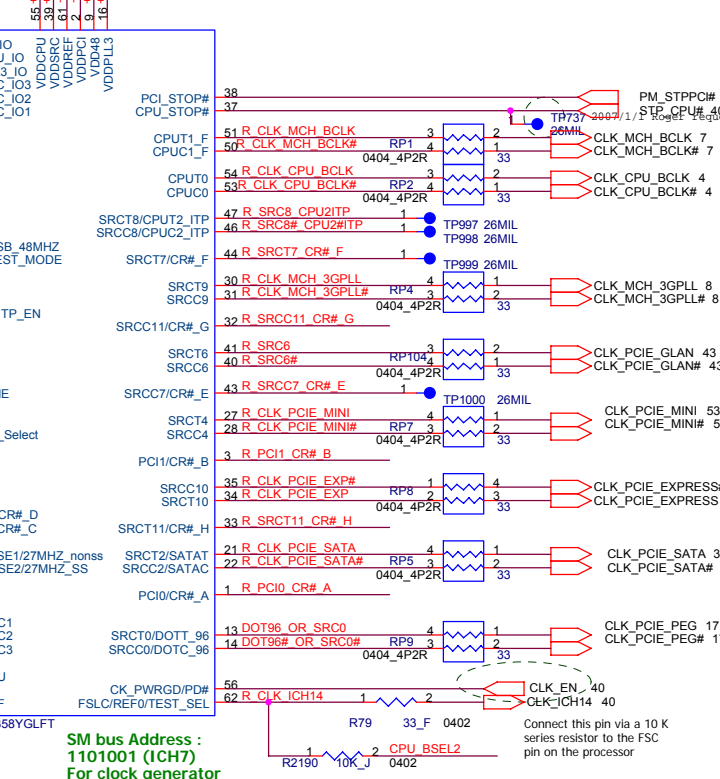
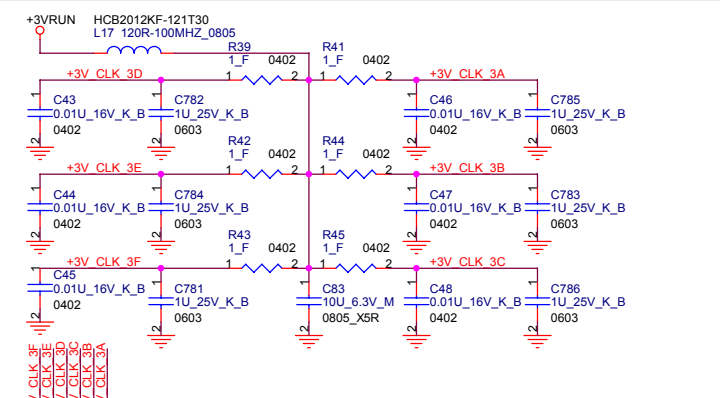


33 MHz Port

Port	M610	MS90
PCI0 (pin1)	NC	NC
PCI1 (pin3)	NC	NC
PCI2 (pin4)	Debug card/EC(KBC)	Debug card
PCI3 (pin5)	PCI8402	PCI8402
PCI4 (pin6)	TV tuner	EC(KBC)
PCI5-F (pin7)	ICH8	ICH8

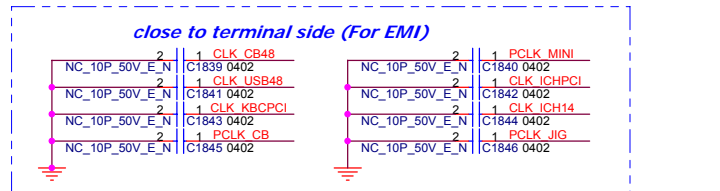
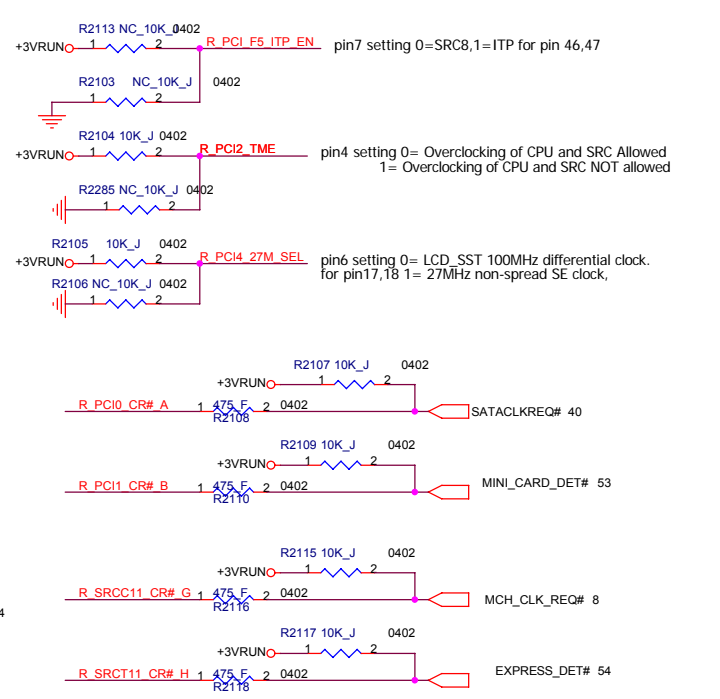
100 MHz Port

Port	M610 setting configuration	S/W Setting this pin type (B2b0=0) for use SRC0	S/W Setting CLKREQ for this pin
SRC0 (pin13,14)	GFX PCIE_PEG		
SRC1 (pin17,18)	(SRC0/SRC1 only either one)		
SRC2 (pin21,22)	PCIE SATA		
SRC3 (pin24,25)	PCIE ICH8		
SRC4 (pin27,28)	PCIE MINI		
SRC6 (pin40,41)	PCIE G-LAN		
SRC7 (pin43,44)	NC		
SRC8 (pin46,47)	NC		
SRC9 (pin30,31)	MCH 3GPLL		
SRC10 (pin34,35)	PCIE EXPRESS		
SRC11 (pin32,33)	CR#G(MCH)/CR#H(EXPRESS)		



FSB Frequency Table:

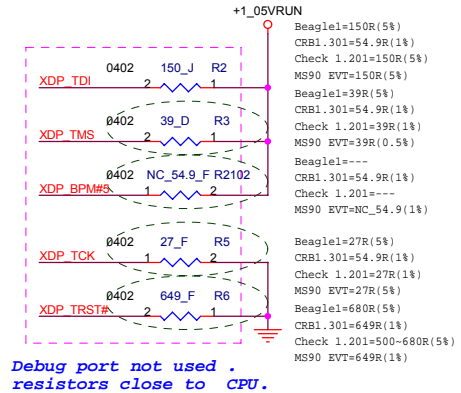
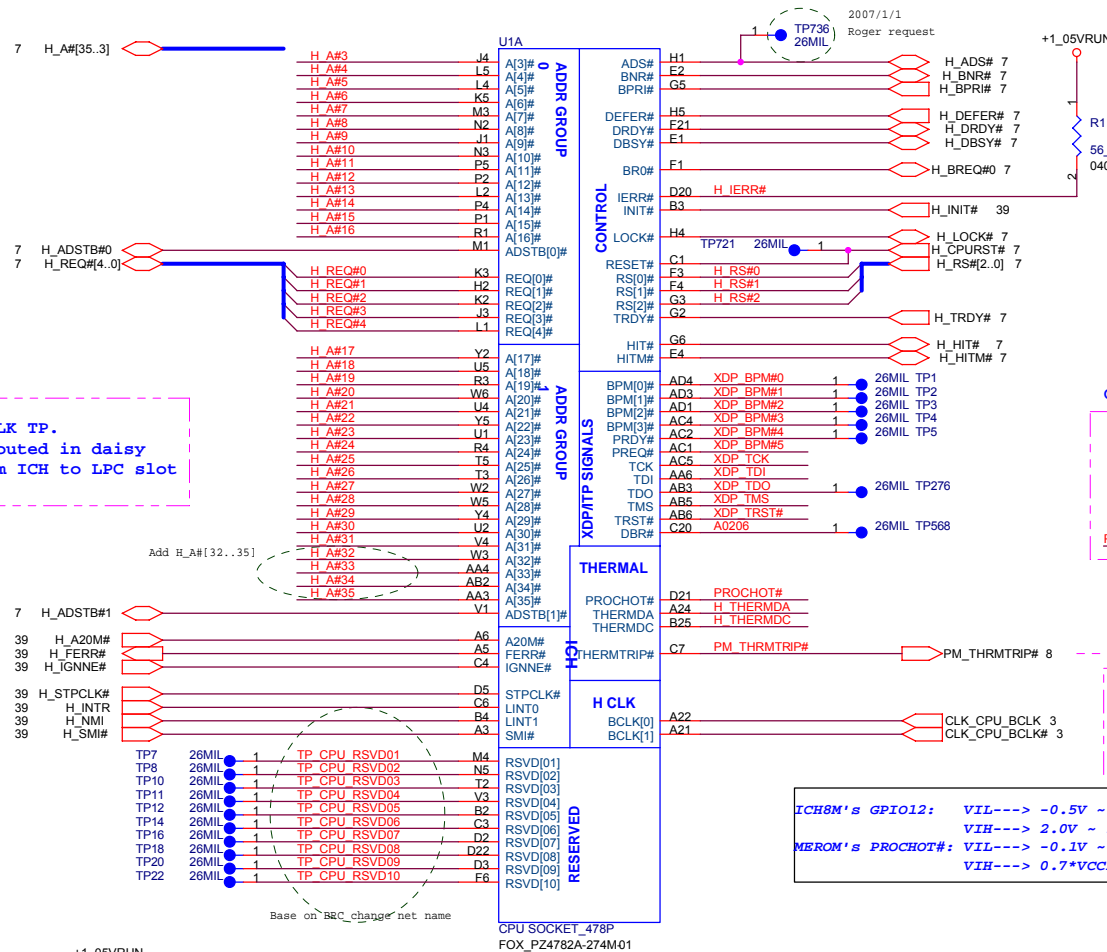
FSLC	FSLB	FSLA	CPU SRC[7:0]	PCI	FSB
1	0	1	100	100	33 /
0	0	1	133	100	33 /
0	1	1	166	100	33 667
0	1	0	200	100	33 800
0	0	0	266	100	33 /
1	0	0	333	100	33 /
1	1	0	400	100	33 /
1	1	1	(Reserved)		



close to terminal side (For EMI)

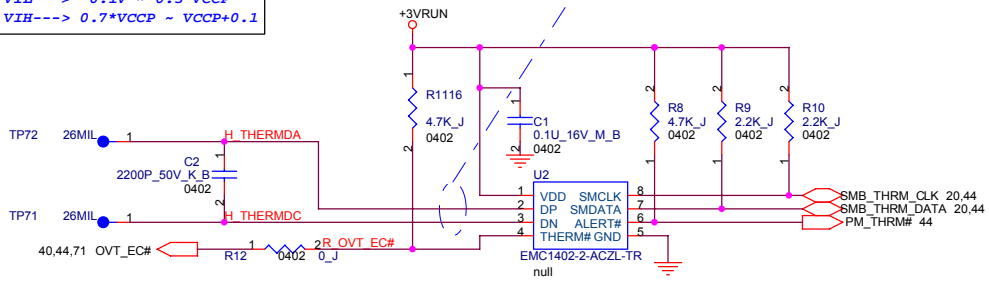
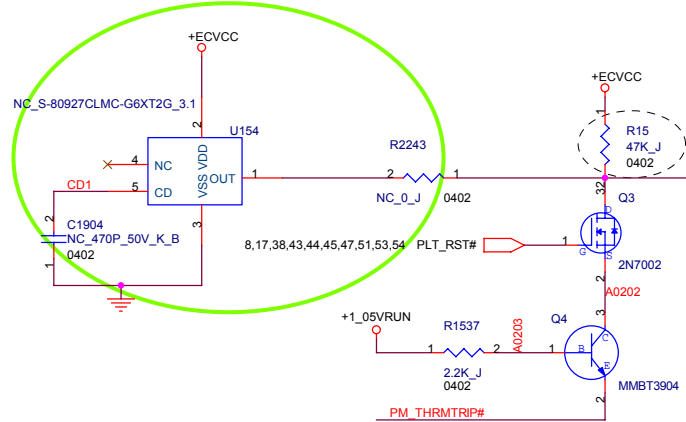
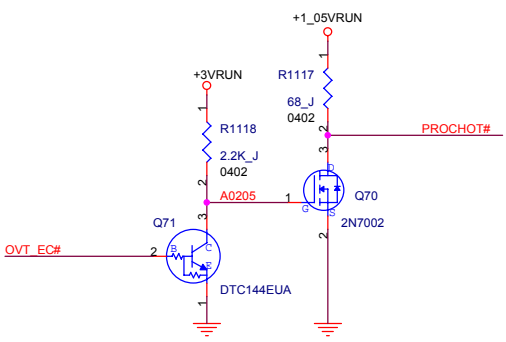
Pin	Component	Value	Pin	Component	Value
1	CLK CB48	0402	1	CLK CB48	0402
2	CLK USB48	0402	2	CLK USB48	0402
3	CLK KBPC1	0402	3	CLK KBPC1	0402
4	CLK ICH14	0402	4	CLK ICH14	0402
5	CLK ICH14	0402	5	CLK ICH14	0402
6	CLK ICH14	0402	6	CLK ICH14	0402
7	CLK ICH14	0402	7	CLK ICH14	0402
8	CLK ICH14	0402	8	CLK ICH14	0402

Layout note:
no stub on H_STPCLK TP.
H_STPCLK# to be routed in daisy chain fashion from ICH7 to LPC slot and then to CPU.



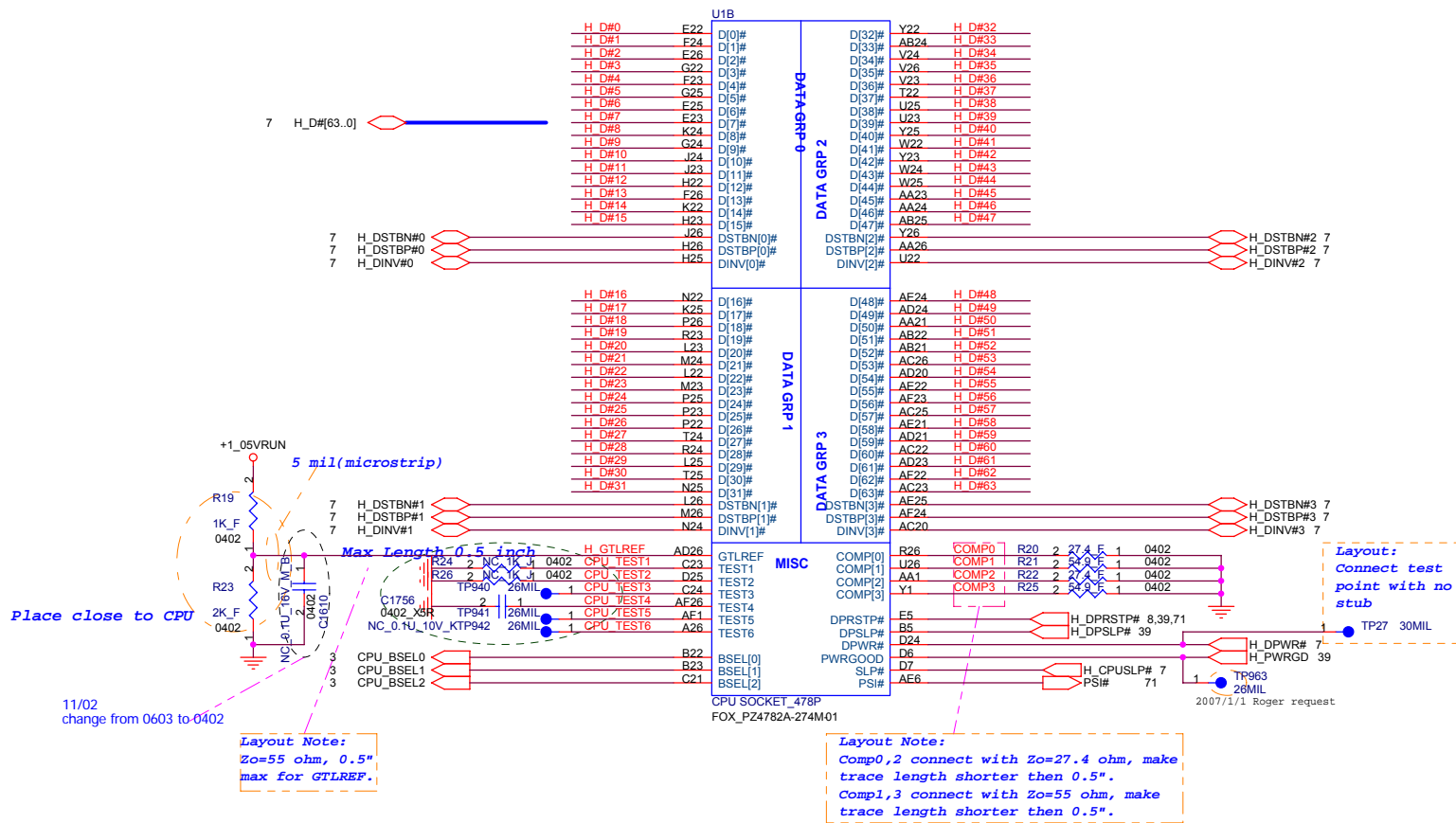
PM_THRMTRIP# should connect to ICH7-M and GMCH without T-ing (No stub)

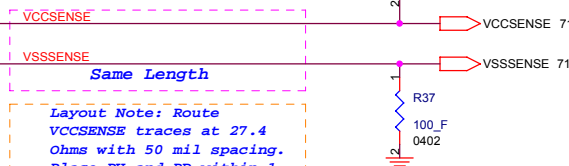
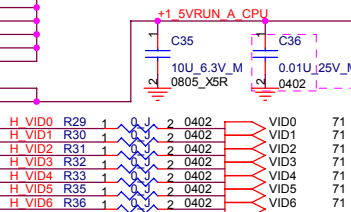
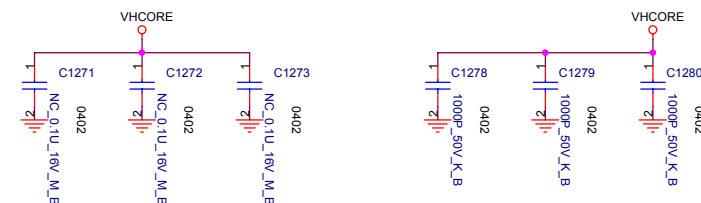
ICH8M's GPIO12: VIL----> -0.5V ~ 0.8V
VHH----> 2.0V ~ 3.3+0.5V
MEROM's PROCHOT#: VIL----> -0.1V ~ 0.3*VCCP
VHH----> 0.7*VCCP ~ VCCP+0.1



SM bus Address :
1001101 = 9A
For F75384M
Place Thermal-Sensor near CPU & GMCH.

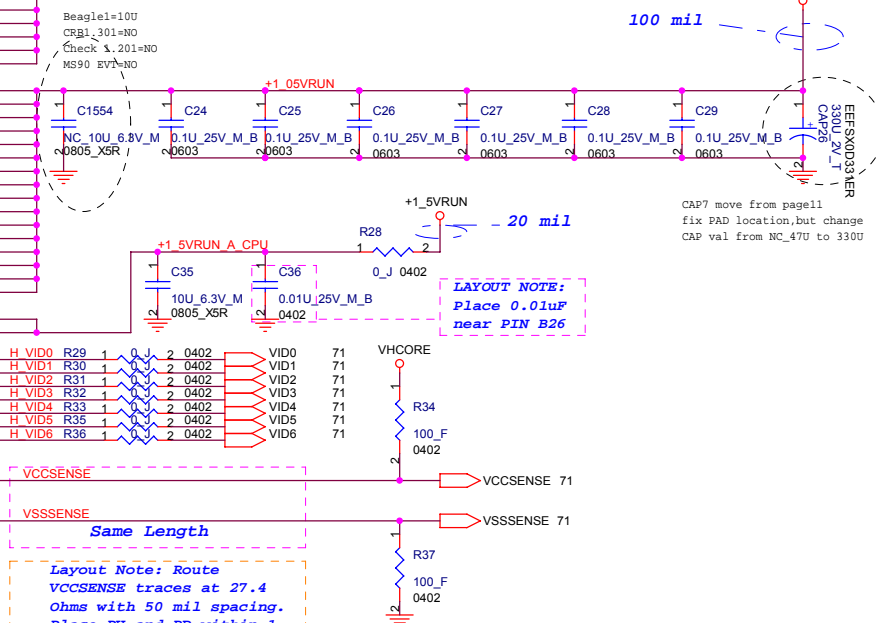
11/16 change part from
F75384M
(15-F75384M-0000) to
G781-1P8F
(15-G7811P8-0000)



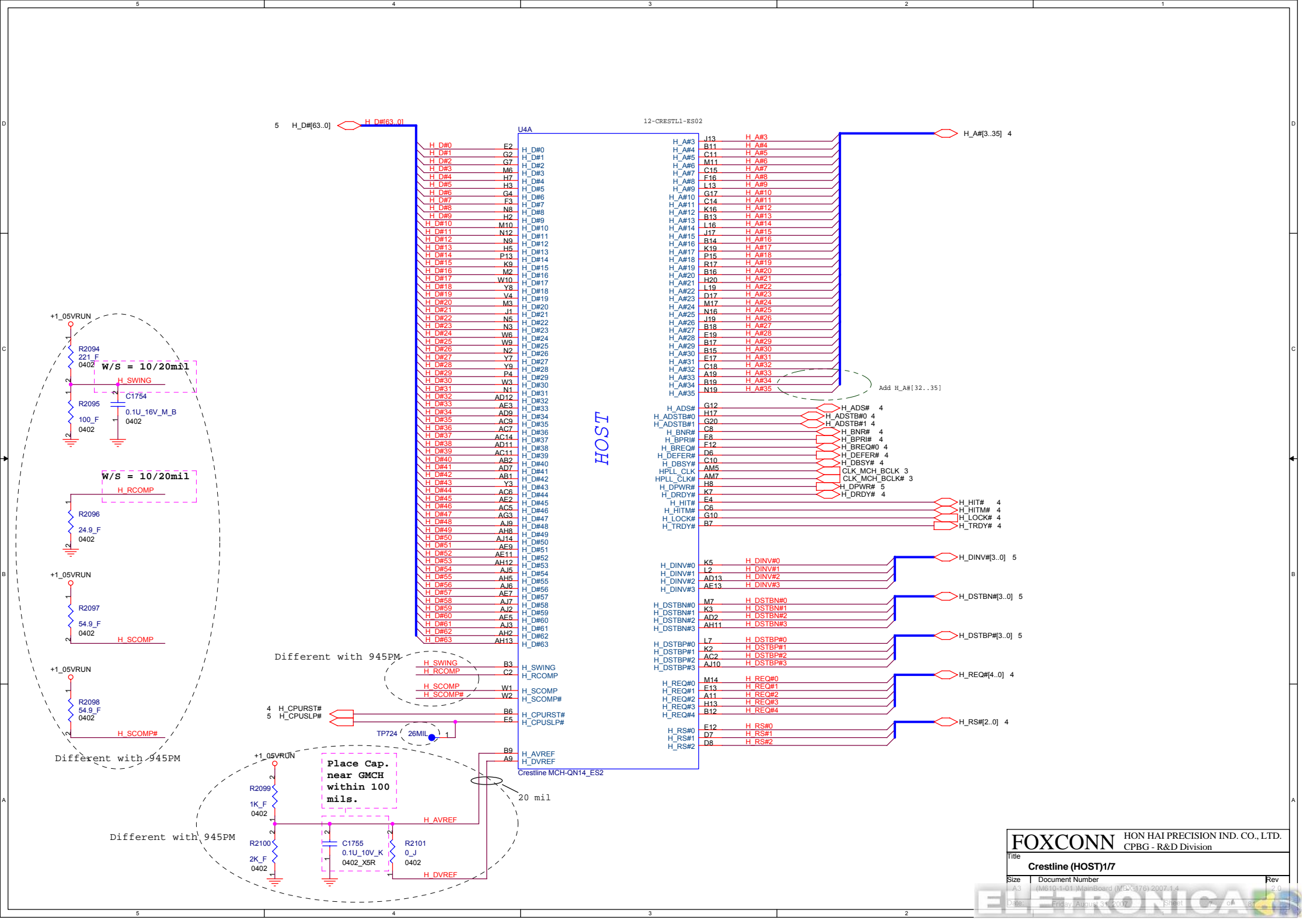


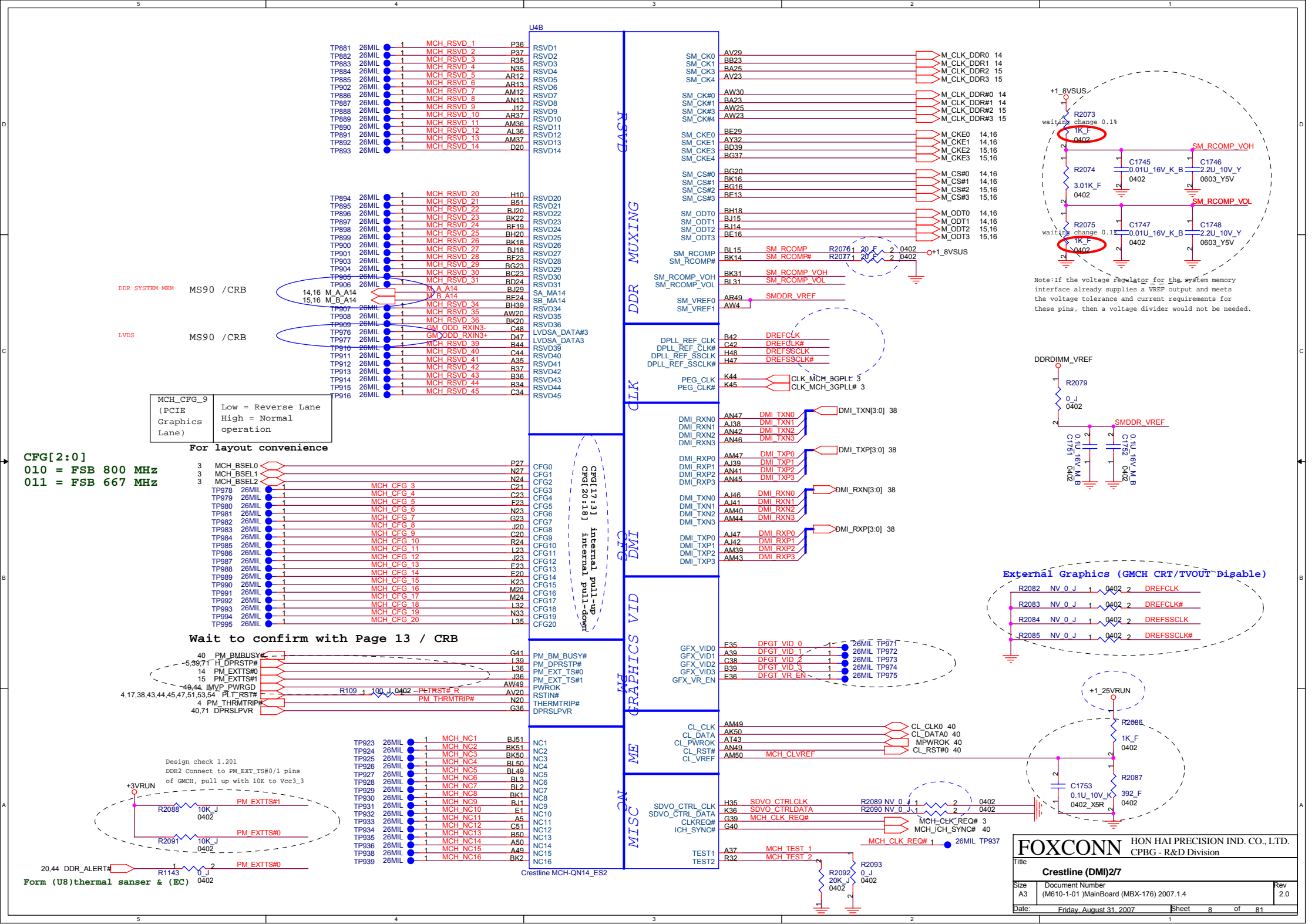
```
width=18 mil
spacing=7 mil
```

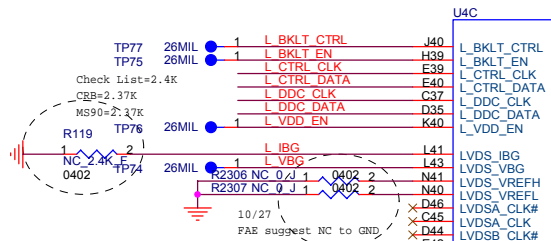
(Design check 1.301) 2006.9.3
No Stuff 27.4 ± 1% pull-down to GND
near Intel MVP 6 controller for testing purposes



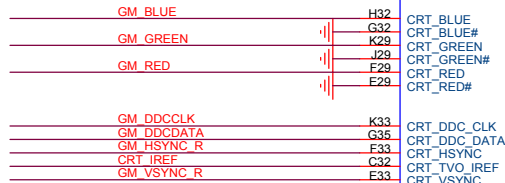
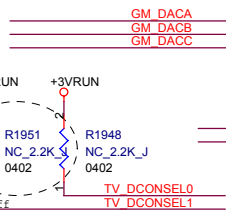
s0 check		UID	
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P11
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
B6	VSS[008]	VSS[089]	T1
B8	VSS[009]	VSS[090]	T4
BE	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B24	VSS[015]	VSS[096]	U24
C5	VSS[016]	VSS[097]	U2
C8	VSS[017]	VSS[098]	V5
C11	VSS[018]	VSS[099]	V22
C14	VSS[020]	VSS[100]	V25
C16	VSS[021]	VSS[101]	W1
C19	VSS[022]	VSS[102]	W4
C2	VSS[023]	VSS[103]	W26
C22	VSS[024]	VSS[104]	Y3
C25	VSS[025]	VSS[105]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E8	VSS[036]	VSS[117]	AA25
E11	VSS[037]	VSS[118]	AB1
E14	VSS[038]	VSS[119]	AB4
E16	VSS[039]	VSS[120]	AB8
E19	VSS[040]	VSS[121]	AB11
E21	VSS[041]	VSS[122]	AB13
E24	VSS[042]	VSS[123]	AB16
F5	VSS[043]	VSS[124]	AB23
F8	VSS[044]	VSS[125]	AB26
F11	VSS[045]	VSS[126]	AC1
F13	VSS[046]	VSS[127]	AC3
F16	VSS[047]	VSS[128]	AC6
F19	VSS[048]	VSS[129]	AC11
F2	VSS[049]	VSS[130]	AC14
F22	VSS[050]	VSS[131]	AC16
F25	VSS[051]	VSS[132]	AC19
G1	VSS[052]	VSS[133]	AC21
G4	VSS[053]	VSS[134]	AC24
G23	VSS[054]	VSS[135]	AD2
G26	VSS[055]	VSS[136]	AD5
H3	VSS[056]	VSS[137]	AD8
H6	VSS[057]	VSS[138]	AD11
H11	VSS[058]	VSS[139]	AD13
H16	VSS[059]	VSS[140]	AD16
H2	VSS[060]	VSS[141]	AD19
J5	VSS[061]	VSS[142]	AD22
J22	VSS[062]	VSS[143]	AD26
J25	VSS[063]	VSS[144]	AE1
K1	VSS[064]	VSS[145]	AE4
K4	VSS[065]	VSS[146]	AE8
K23	VSS[066]	VSS[147]	AE11
K26	VSS[067]	VSS[148]	AE14
L3	VSS[068]	VSS[149]	AE16
L6	VSS[069]	VSS[150]	AE19
L21	VSS[070]	VSS[151]	AE23
L24	VSS[071]	VSS[152]	AE26
M2	VSS[072]	VSS[153]	A2
M5	VSS[073]	VSS[154]	AF6
M22	VSS[074]	VSS[155]	AF11
M25	VSS[075]	VSS[156]	AF13
N1	VSS[076]	VSS[157]	AF16
N4	VSS[077]	VSS[158]	AF19
N13	VSS[078]	VSS[159]	AF21
N23	VSS[079]	VSS[160]	A25
N26	VSS[080]	VSS[161]	AF25
P3	VSS[081]	VSS[162]	
		VSS[163]	



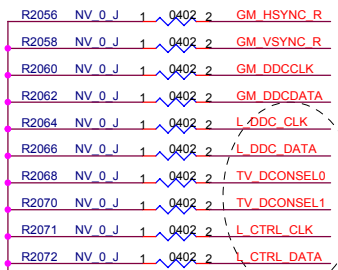
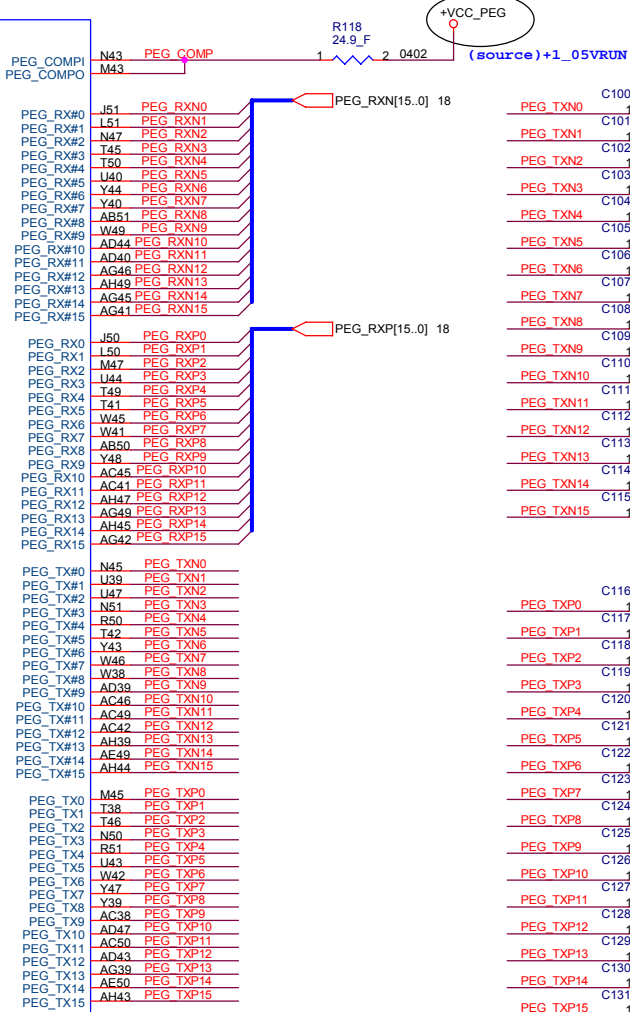
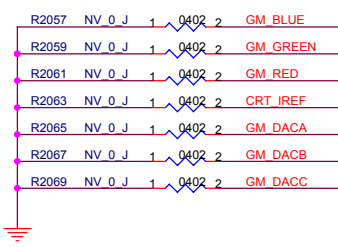




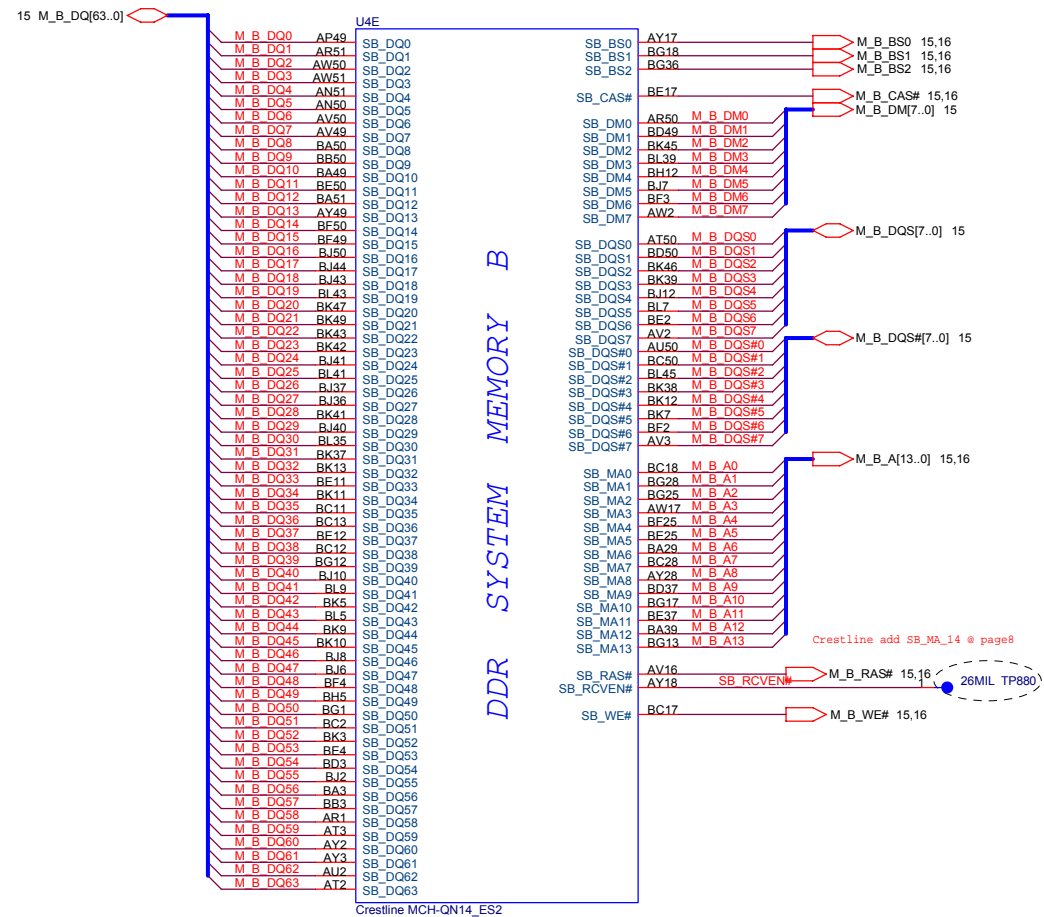
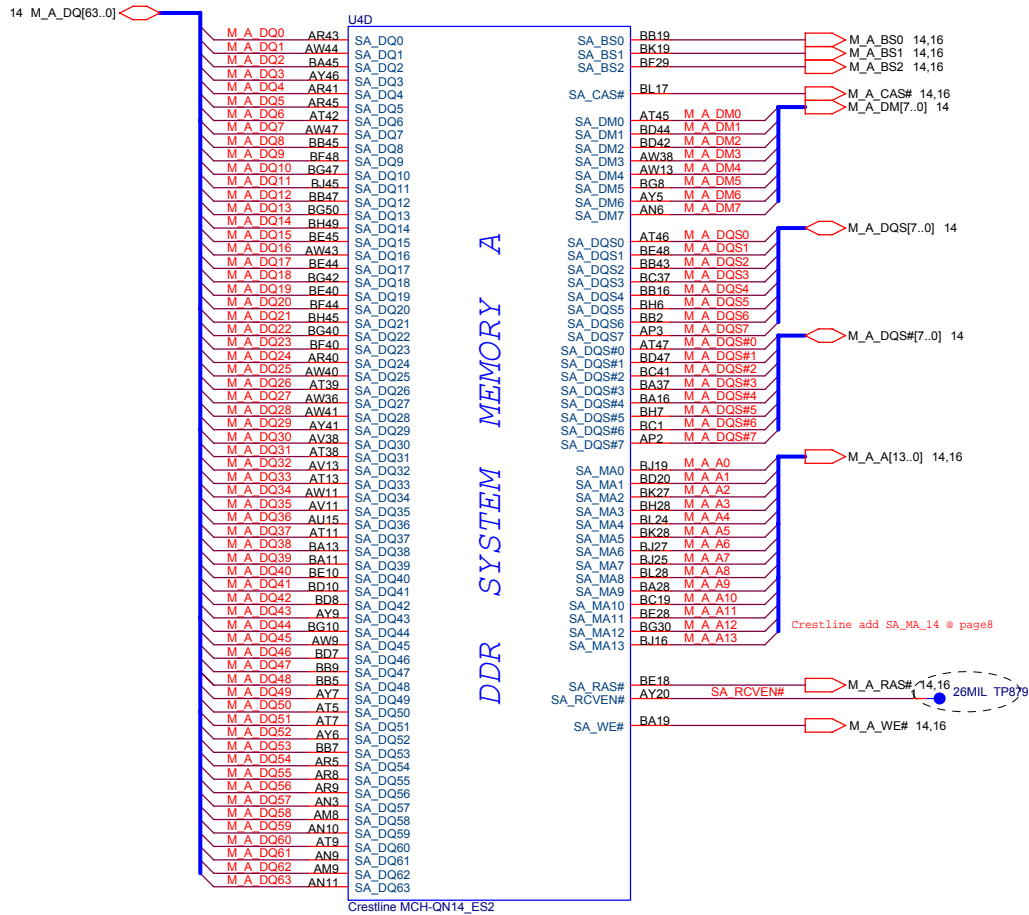
TYPE is open drawn(Output)
Check list 2.2K to 3.3V
MS90 2.2K to 3.3V
CRB 2.2K to 3.3V
10/27
Change NC to stuff

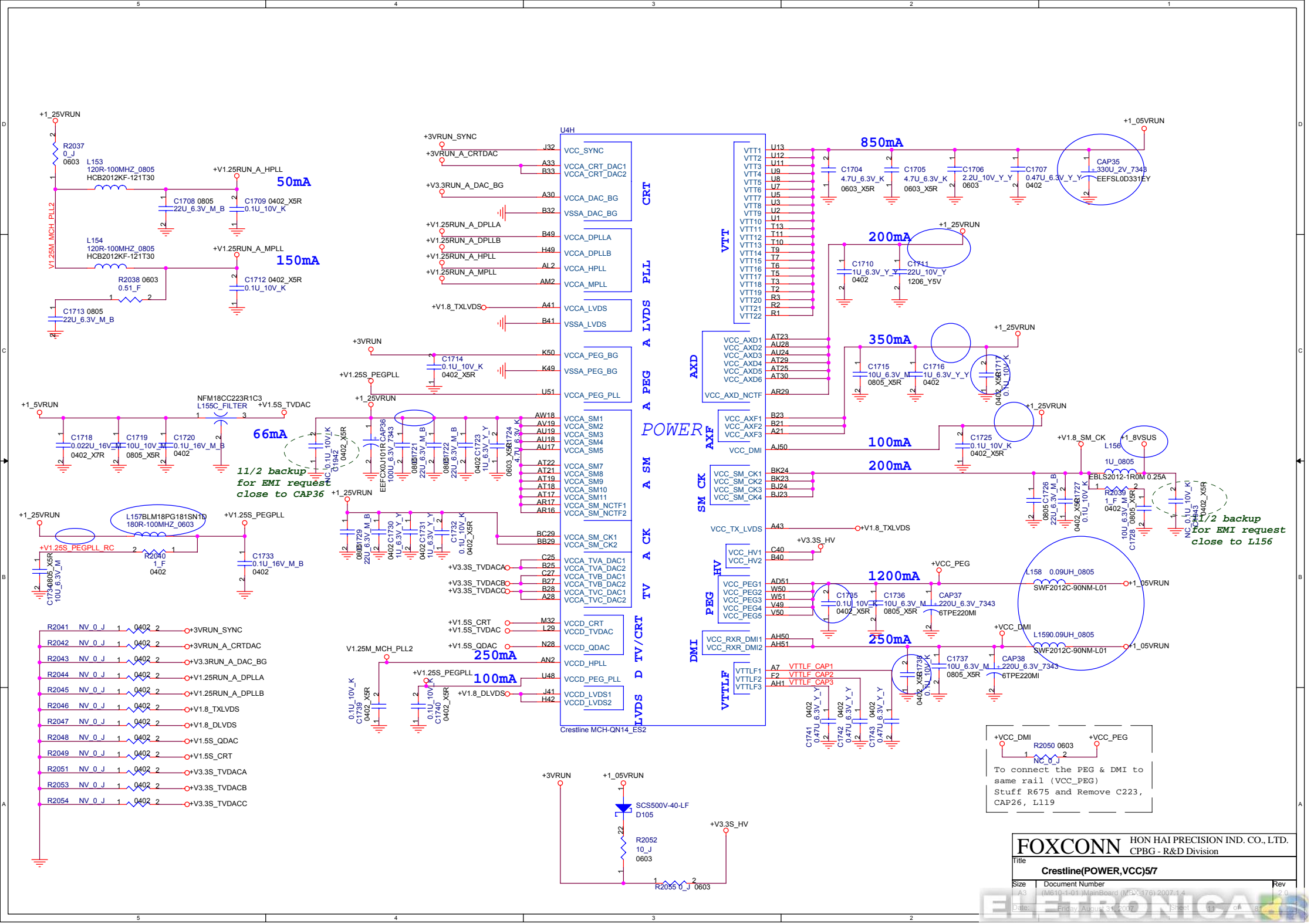


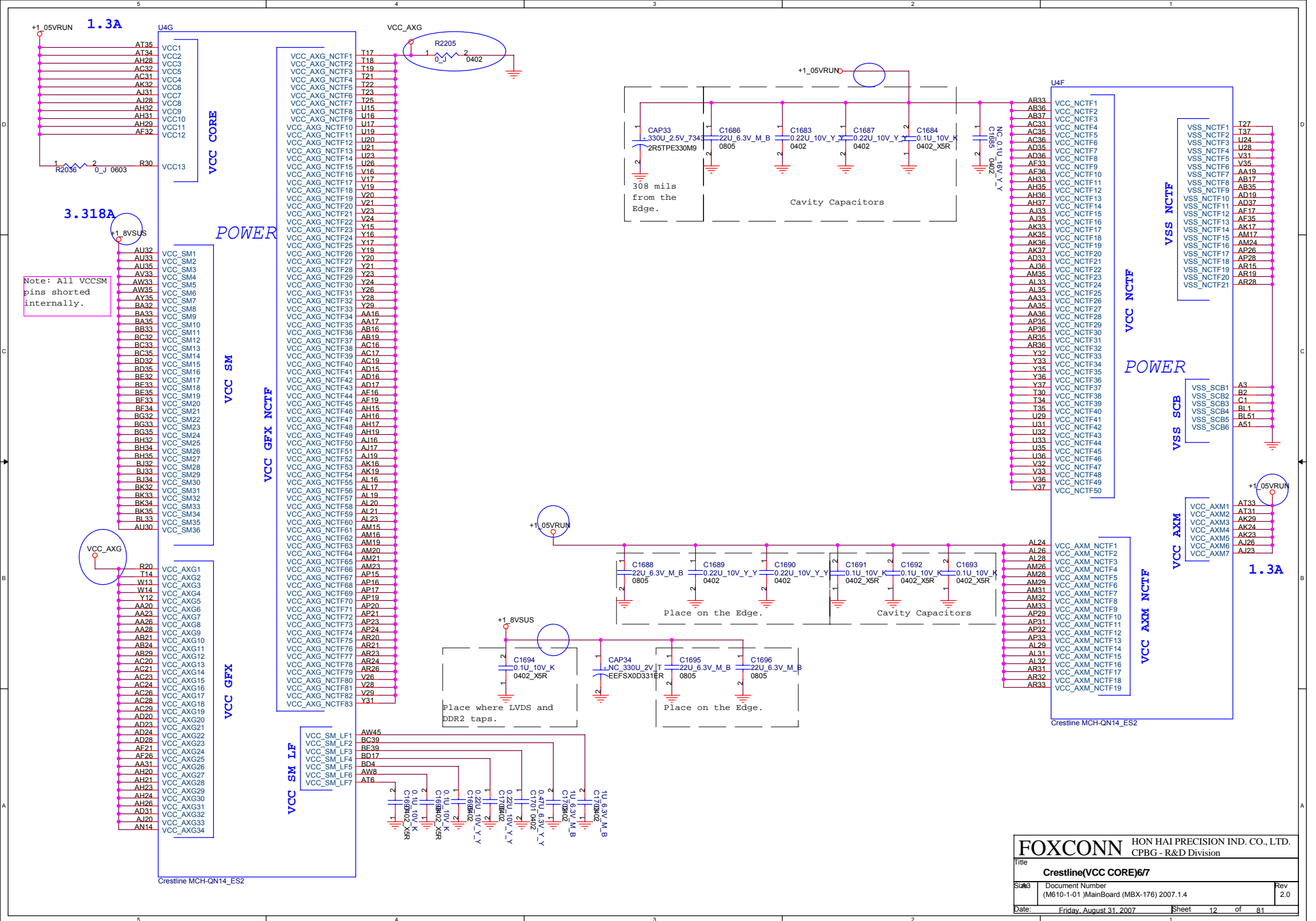
External Graphics (GMCH CRT/TVOUT Disable)

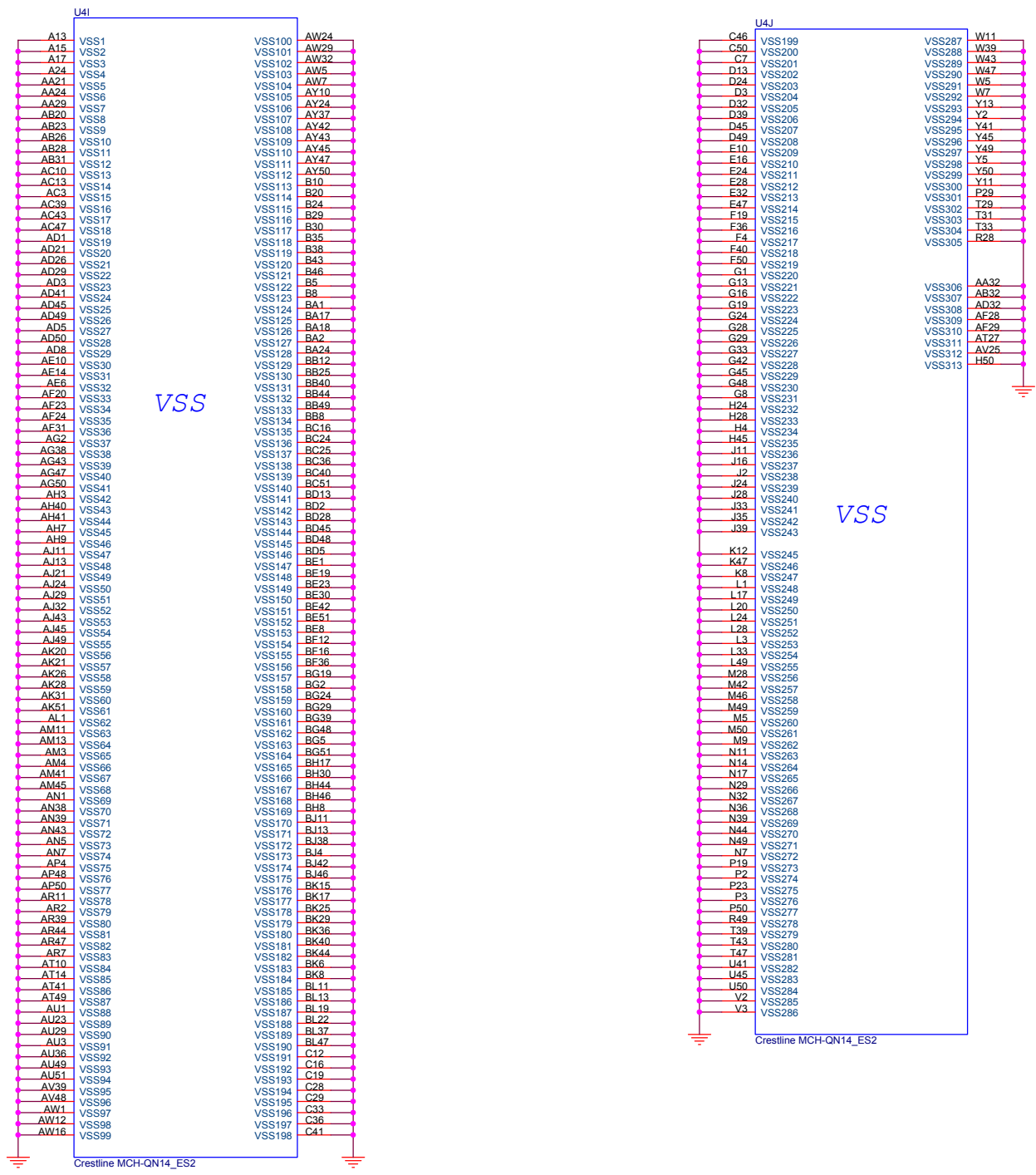


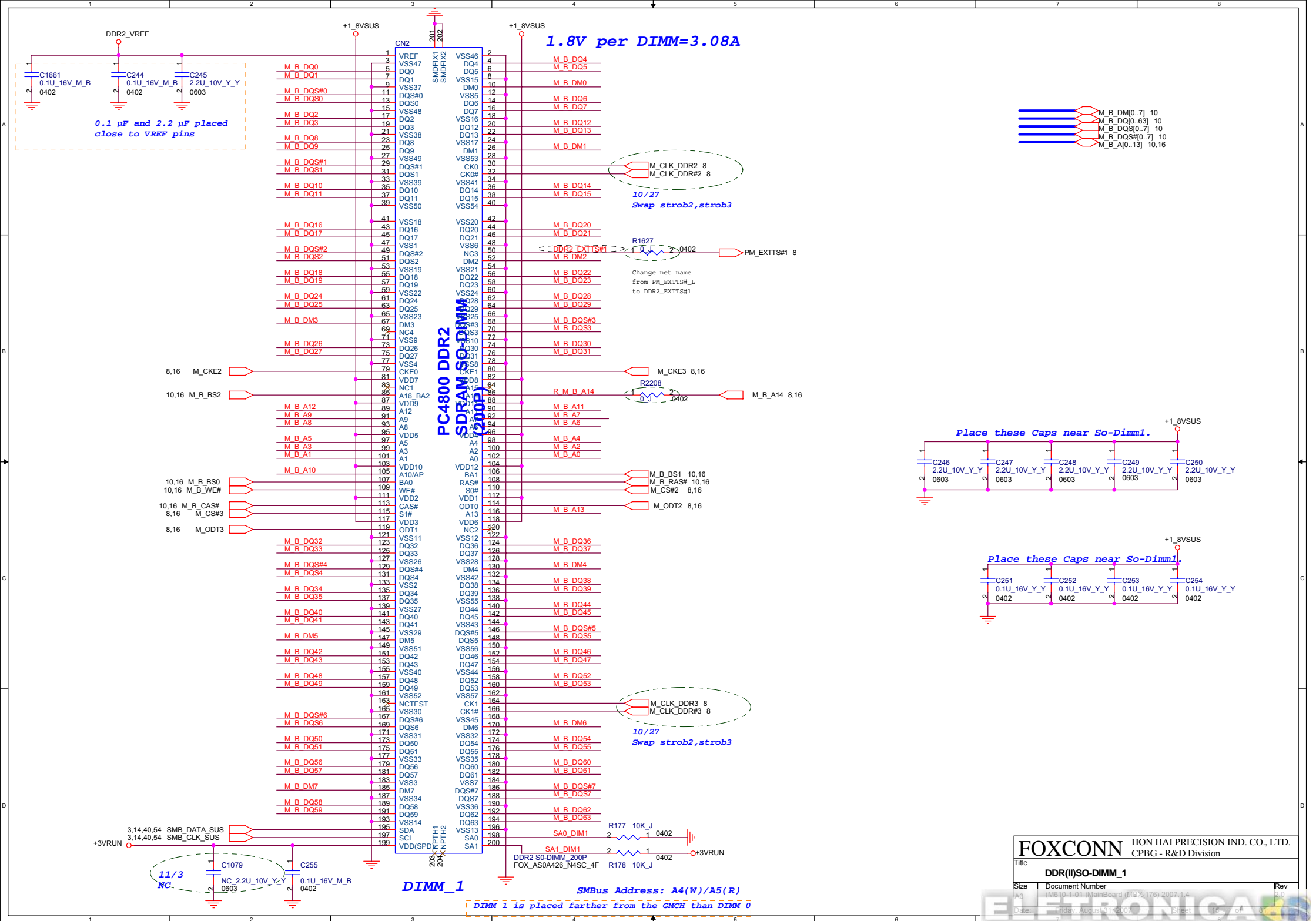
Base on below document:
Mobile Merom Processor and Crestline Chipset
- Santa Rosa Platform Design Guide-21112,1.0
.pvd.pdf (May 2006/ Rev 1.0)page 193
Table 82. External Graphics (GMCH Integrated Graphics Disable)
Connect these signals to GND

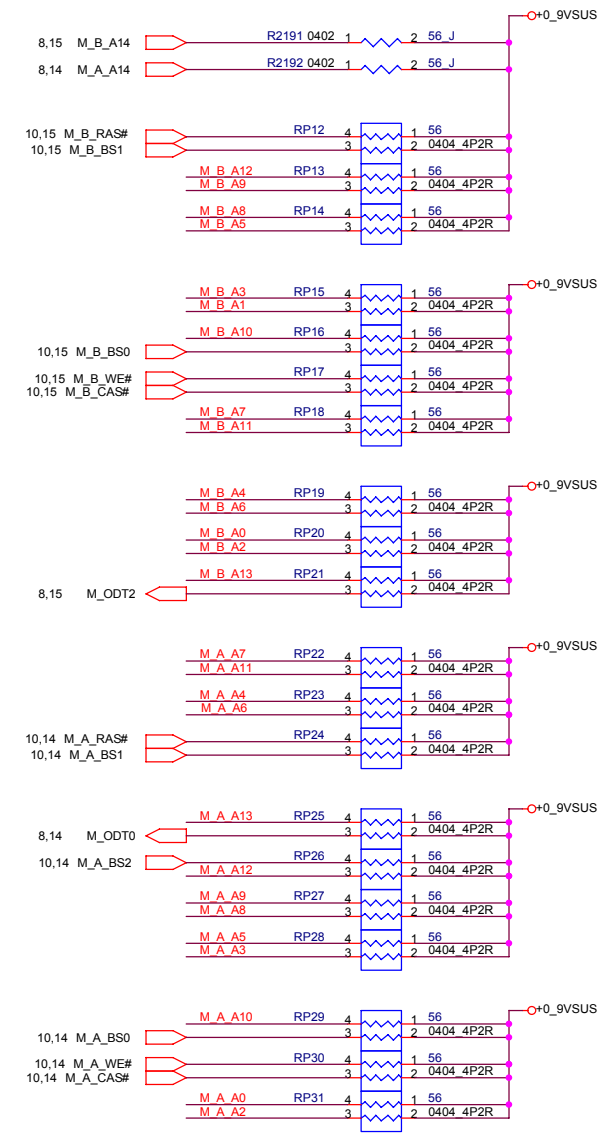
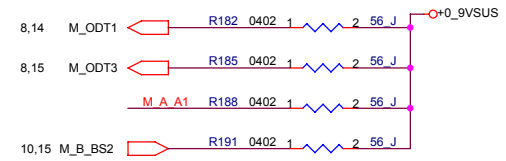
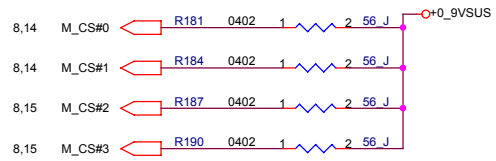
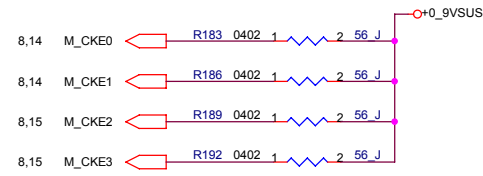
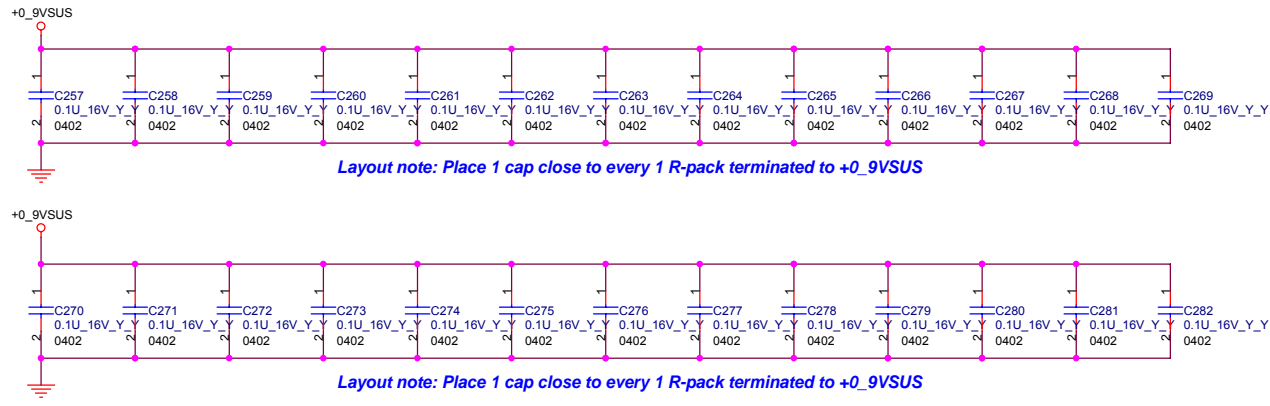


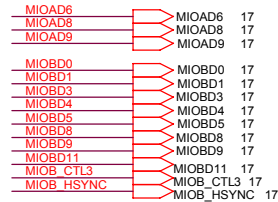
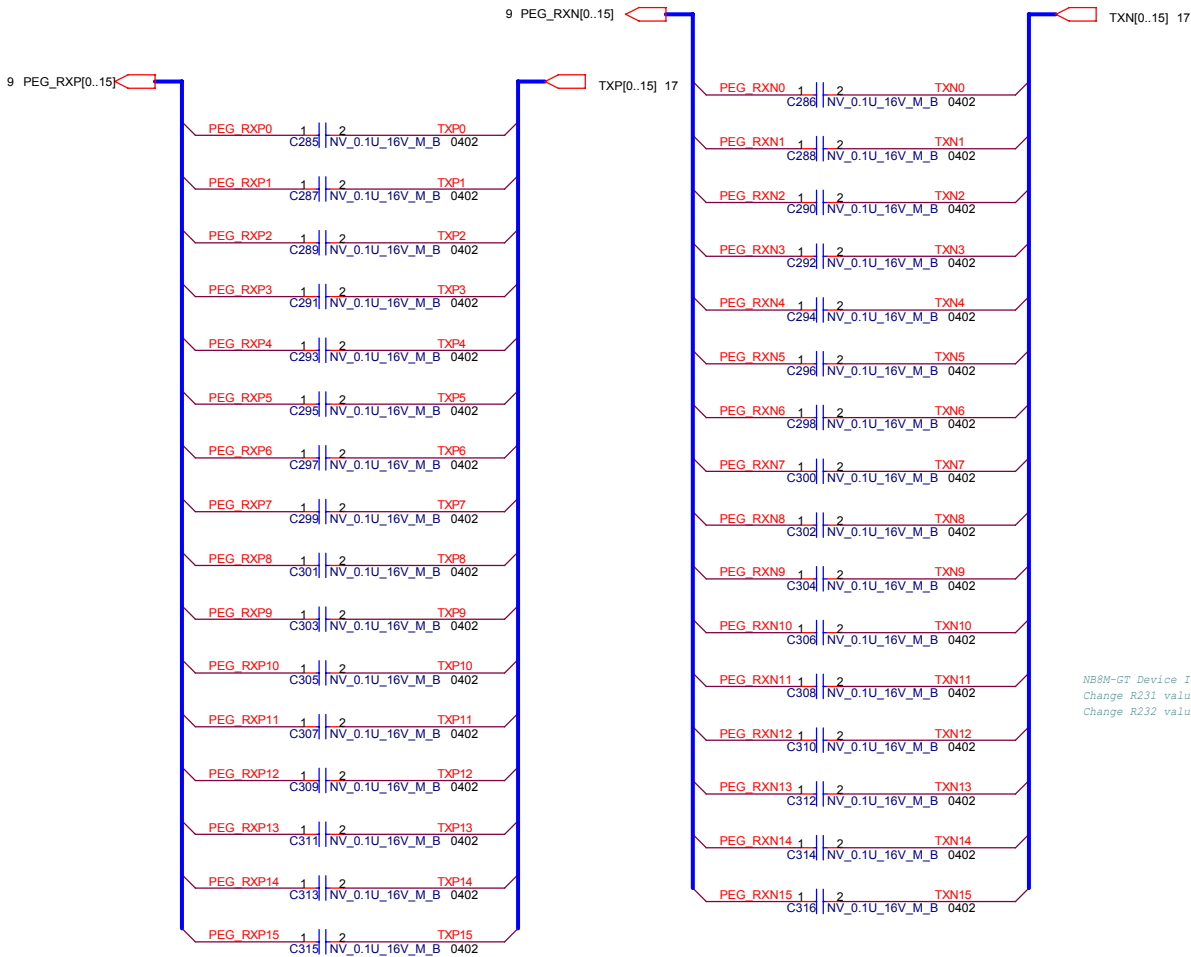












NB8X Strap for GDDR3-136ball RAM_CFG0

0001 16Mx32Infineon
0010 16Mx32Hynix
0011 16Mx32Samsung
0101 8Mx32Infineon
0110 8Mx32Hynix
0111 8Mx32Samsung

SUB_VENDOR

0 (USE SYSTEM BIOS)
1 (USE EXTERNAL ROM)

MIOAD0 is used to set the PCI Express PLL termination enable.

DEFAULT "0"

NB8X 3GIO_PADCFG[3:0]

0001

NB8M-GT Device ID setting mismatch between VBIOS and H/W Straps
Change R231 value from NC_ to NV8M_
Change R232 value from NV_ to NV8P_

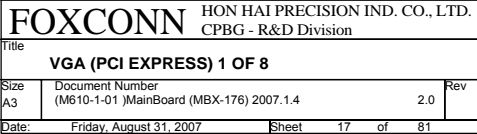
NB8X PCI_DEVID[4:0]

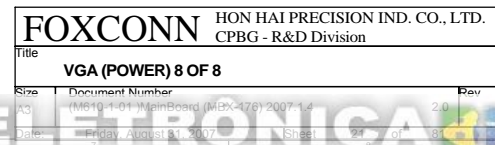
NB8P-GS X0111 "X7"
NB8M-GT X0110 "X6"

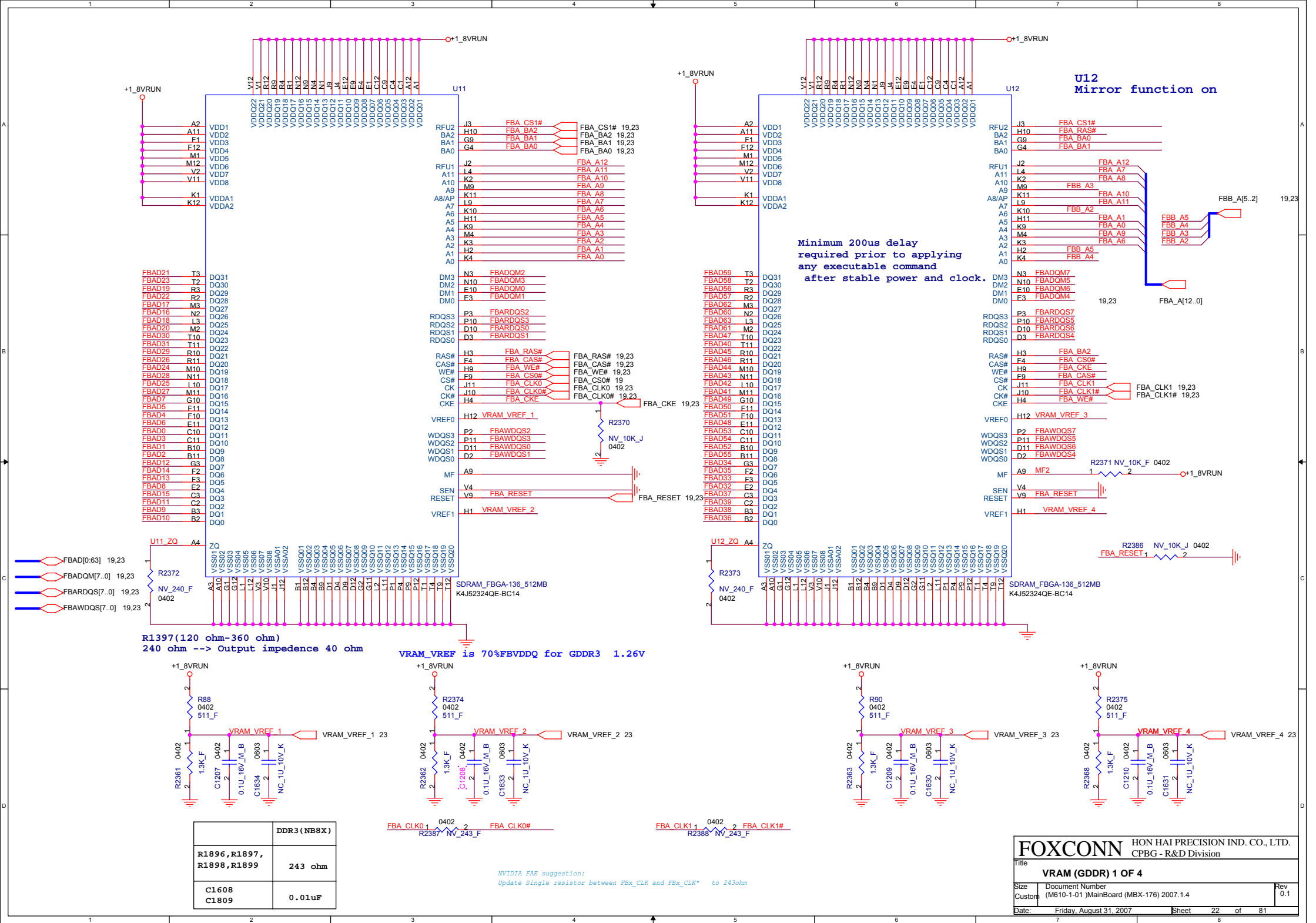
CRYSTAL(NB8X)

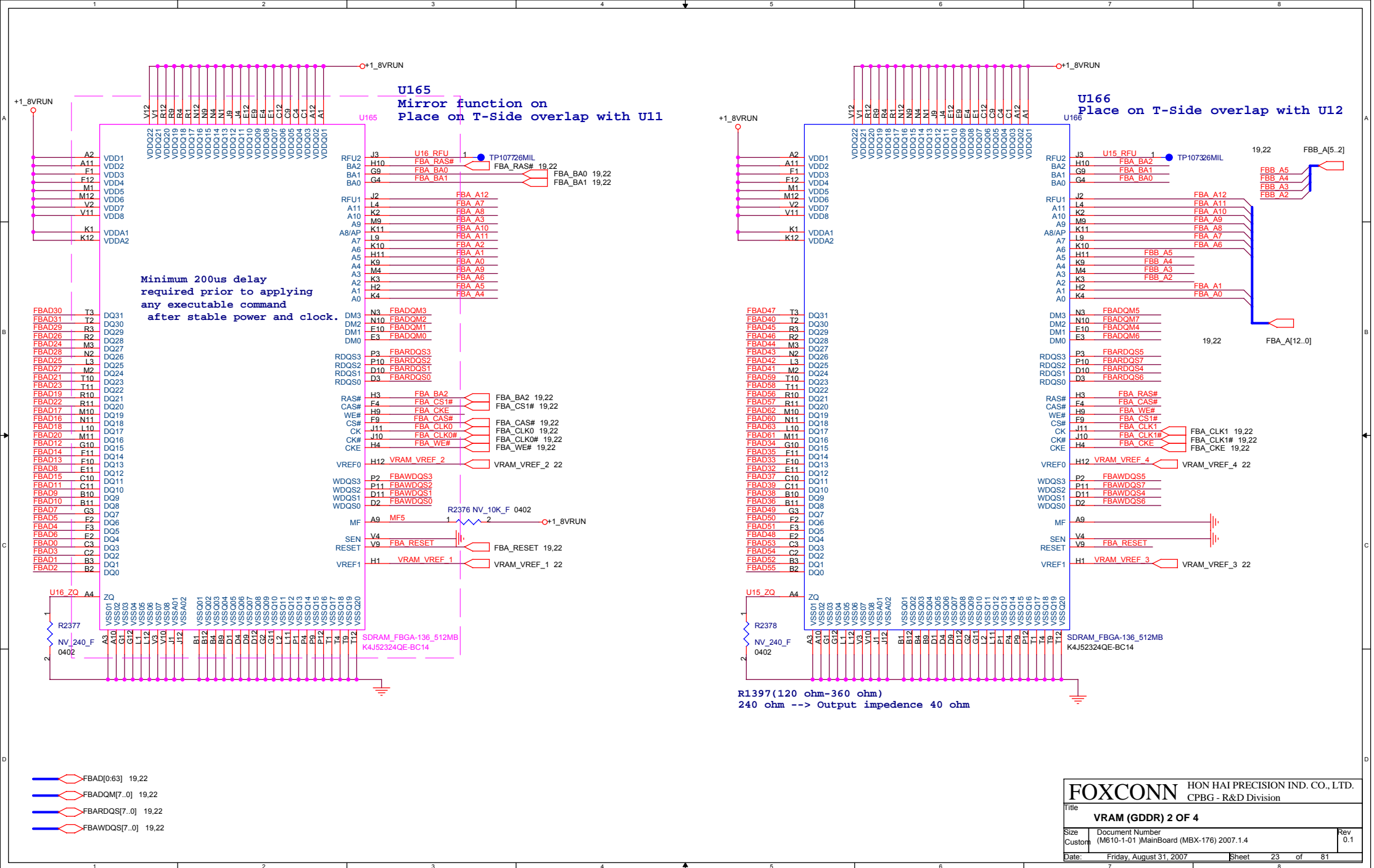
0 (27M Hz)
1 (Reserved)

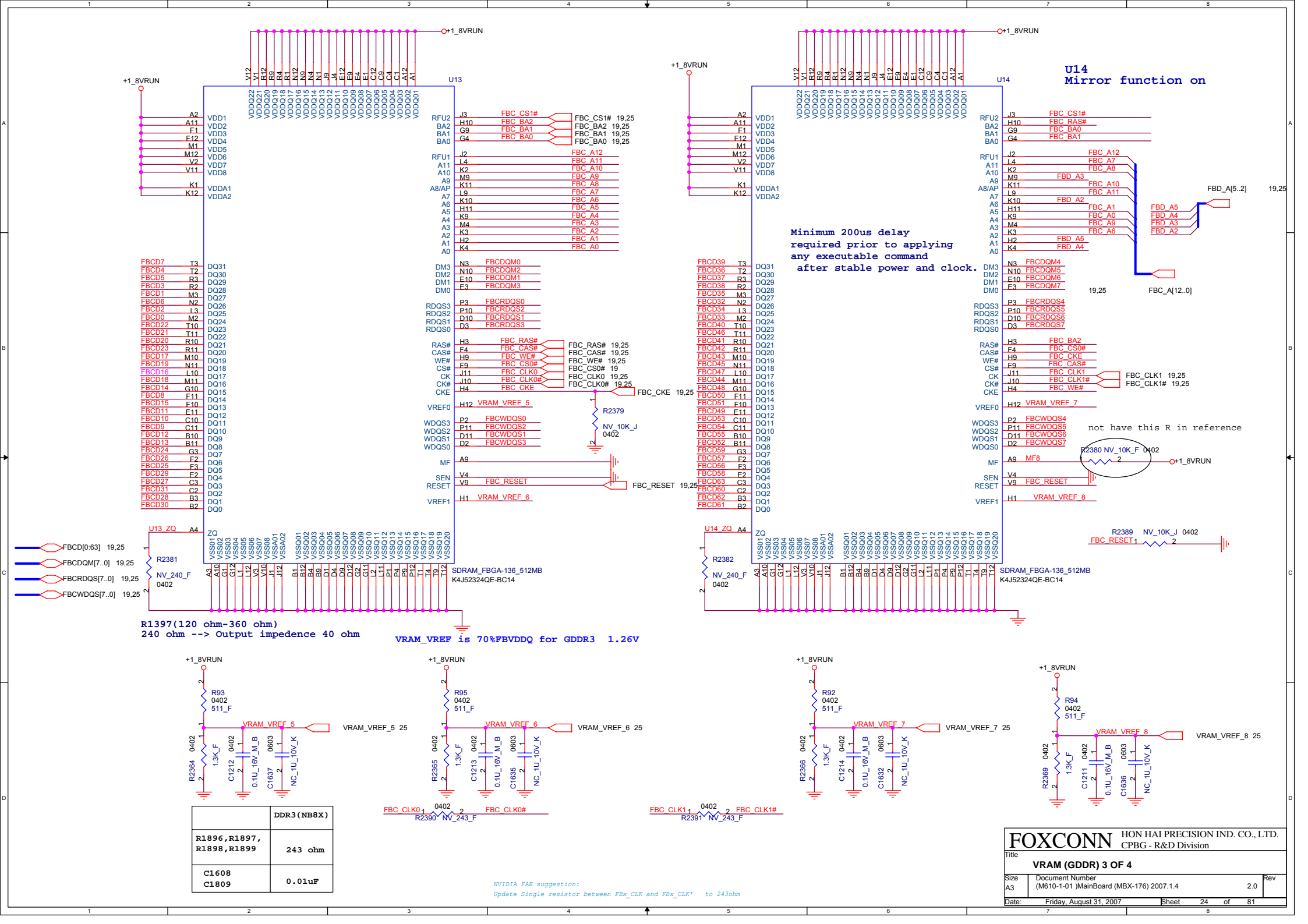


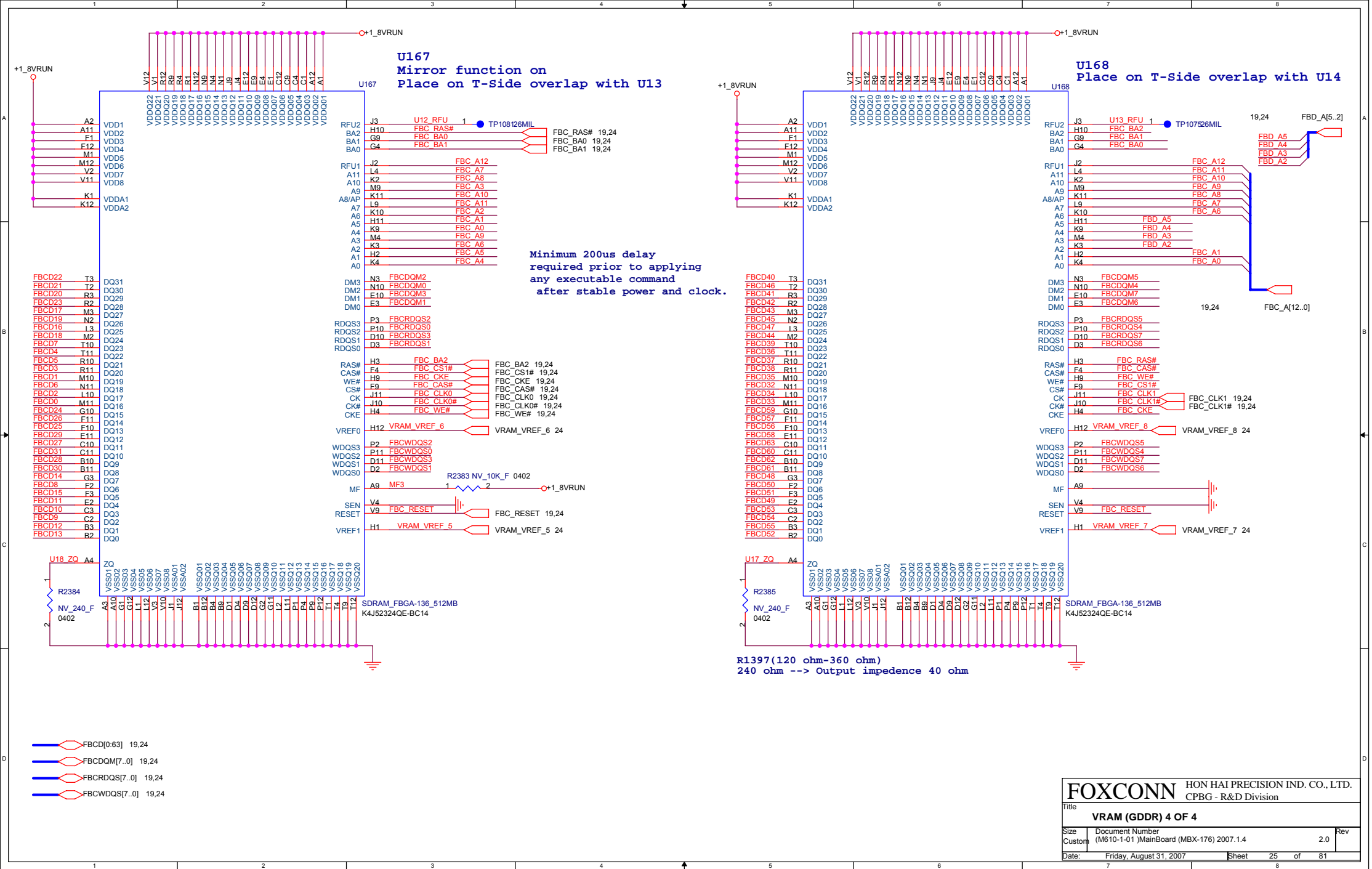












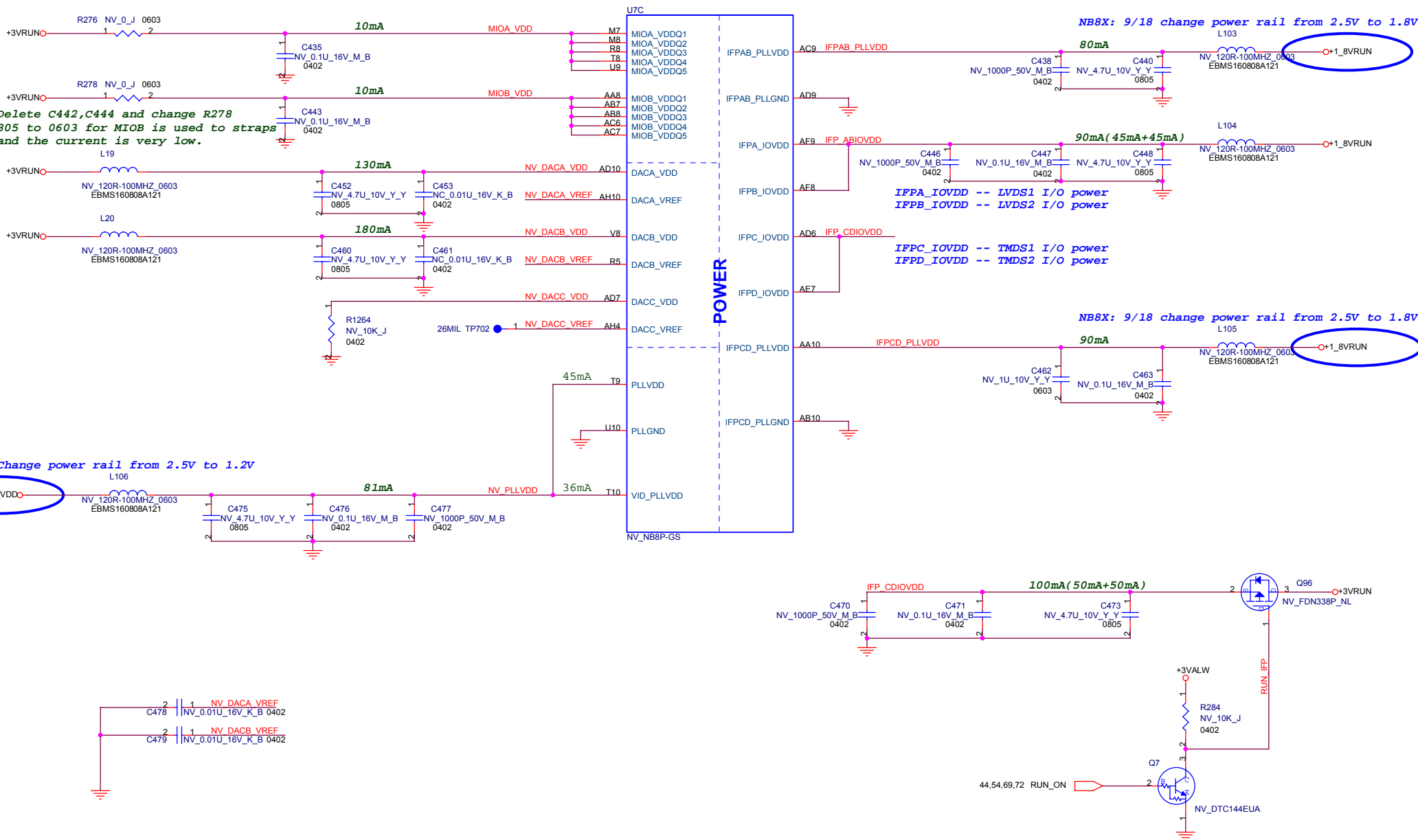
10/17 Delete C442,C444 and change R278 from 0805 to 0603 for MIOB is used to straps input and the current is very low.

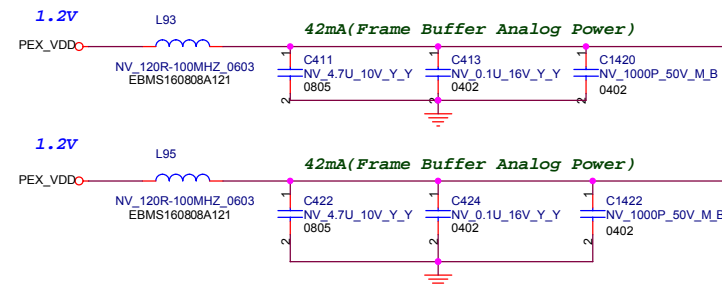
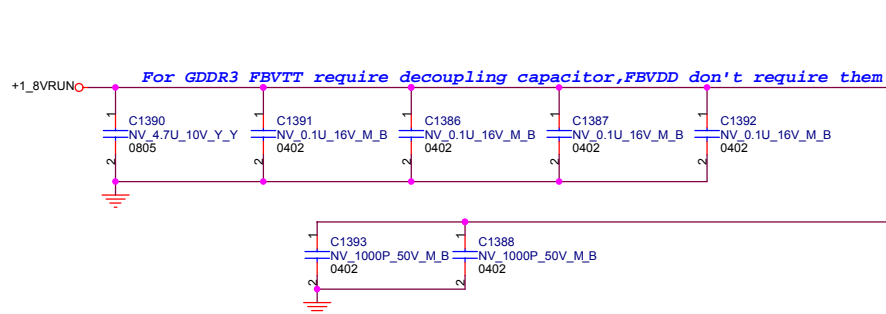
NB8X: Change power rail from 2.5V to 1.2V

NB8X: 9/18 change power rail from 2.5V to 1.8V

NB8X: 9/18 change power rail from 2.5V to 1.8V

POWER





FBCAL_PD_VDDQ K26

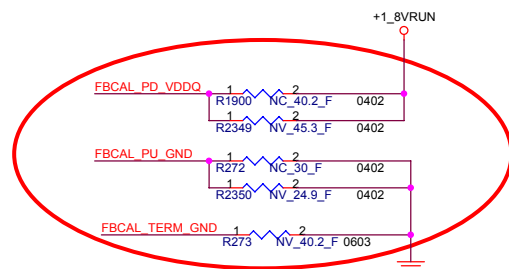
FBCAL_PU_GND H26

FBCAL_TERM_GND J26

FBCAL_PD_VDDQ

FBCAL_PU_GND

FBCAL_TERM_GND



NVIDIA update NB8M VRAM termination value

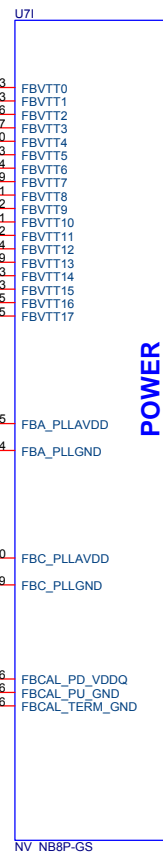
FBCAL_PD_VDDQ 45.3 Ω

FBCAL_PU_GND 24.9 Ω

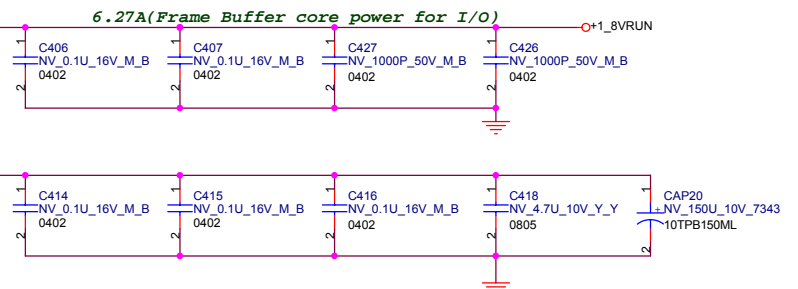
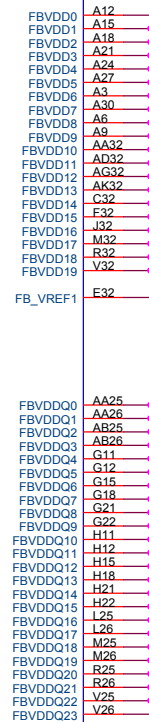
FBCAL_TERM_GND 40.2 Ω

NVIDIA 07/1/5 update

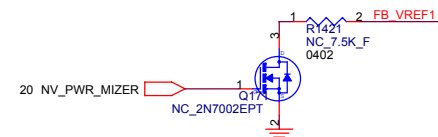
	DDR3(NB8M-GT)	DDR3(NB8P-GS)
FBCAL_PD_VDDQ	45.3 ohm	45.3 ohm
FBCAL_PU_GND	24.9 ohm	24.9 ohm
FBCAL_TERM_GND	40.2 ohm	40.2 ohm



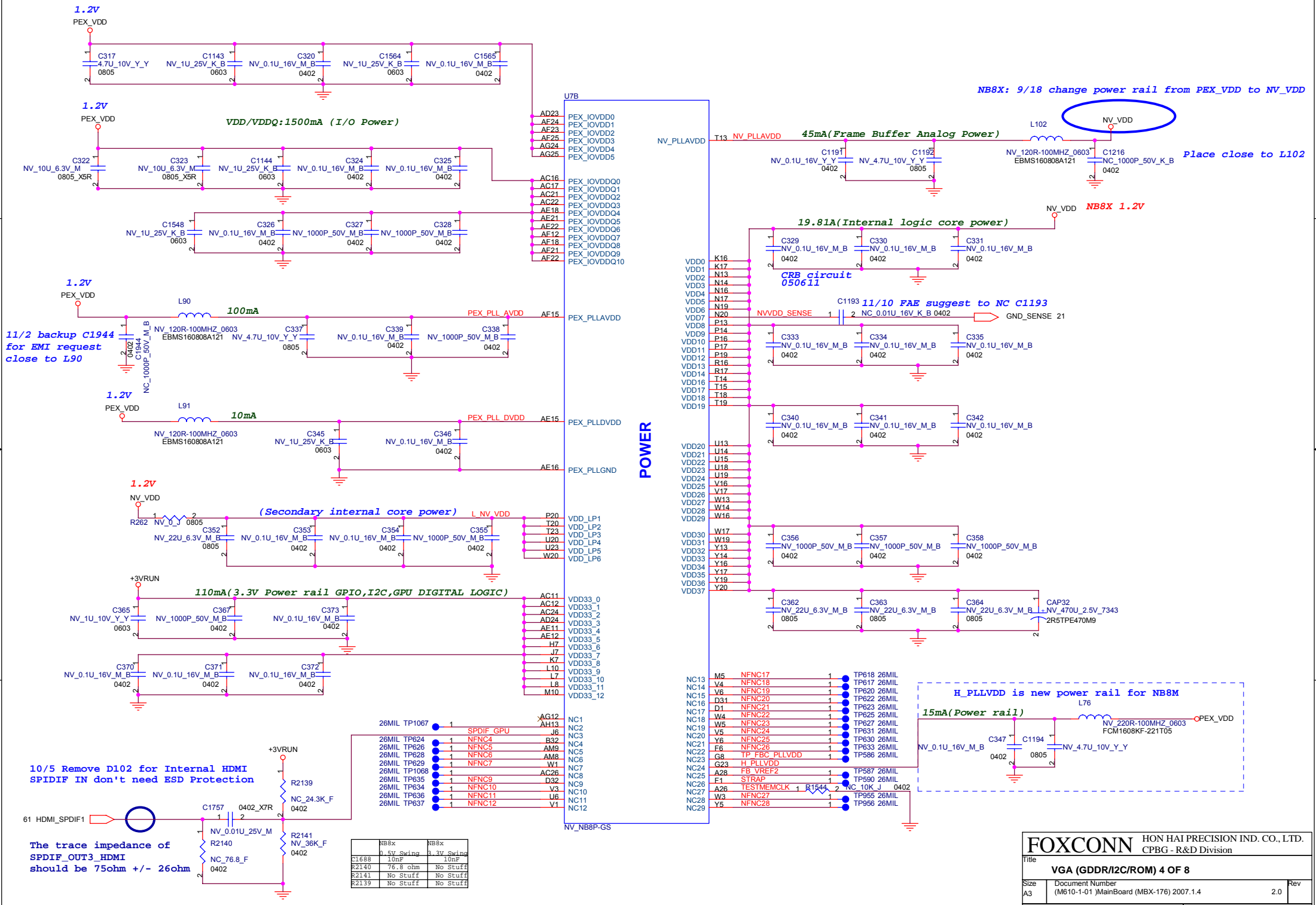
POWER



10/18 Replace CAP20 by a higher ESR cap(40mohm) for cost down

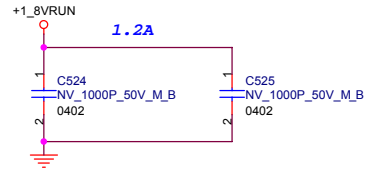
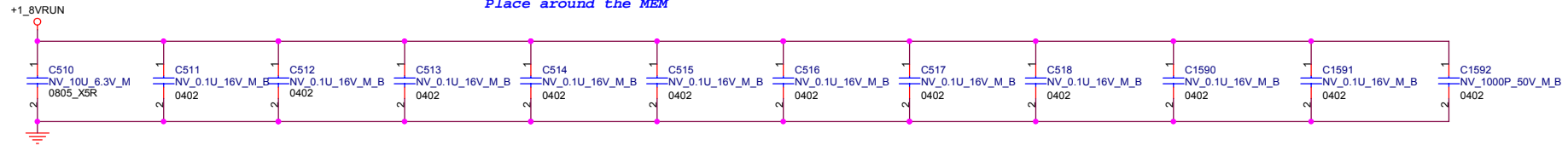


Memory Vref switch controlled by GPIO10



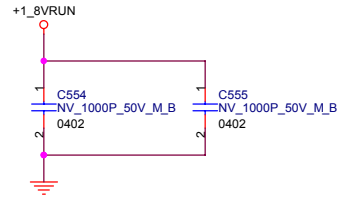
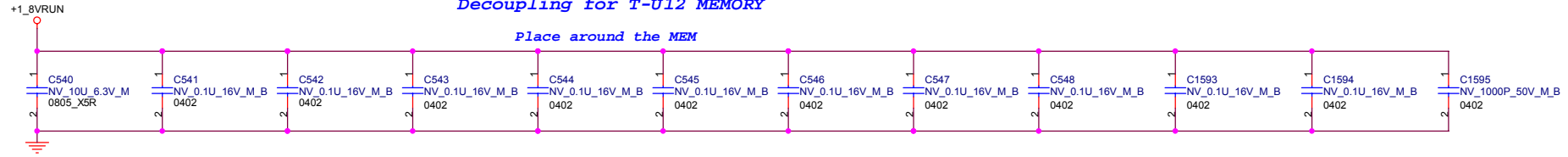
Decoupling for T-U11 MEMORY

Place around the MEM



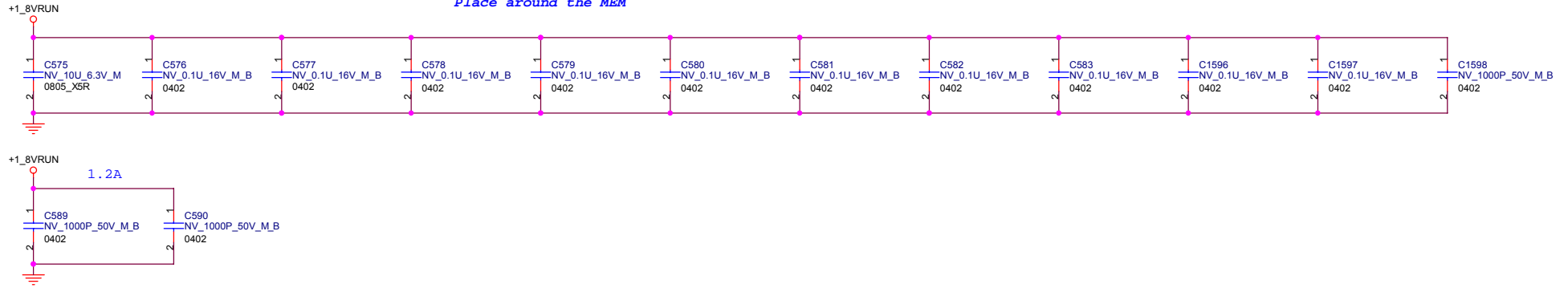
Decoupling for T-U12 MEMORY

Place around the MEM



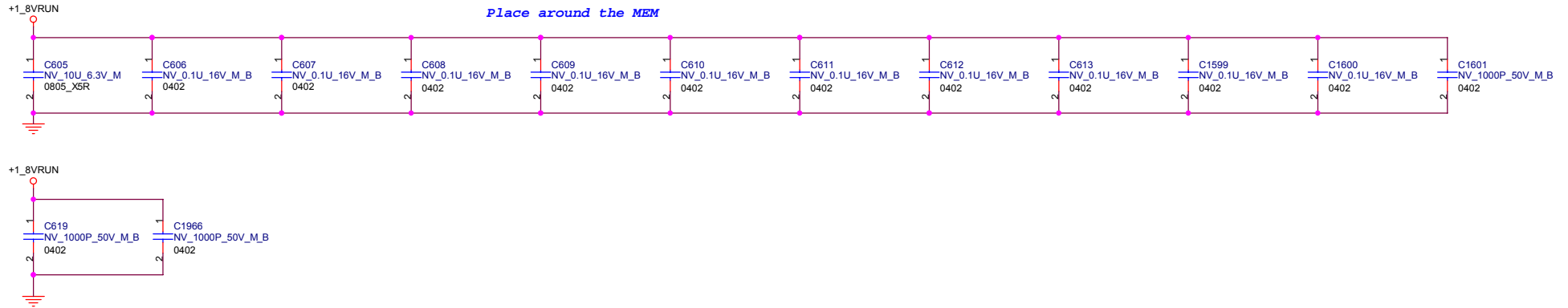
Decoupling for T-U13 MEMORY

Place around the MEM



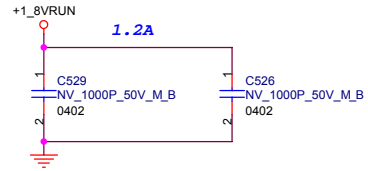
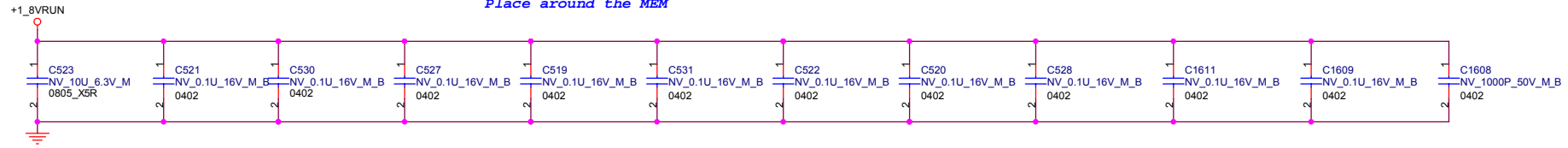
Decoupling for T-U14 MEMORY

Place around the MEM



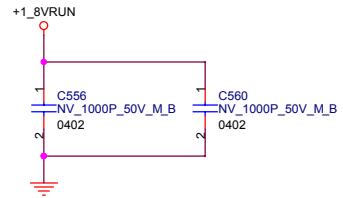
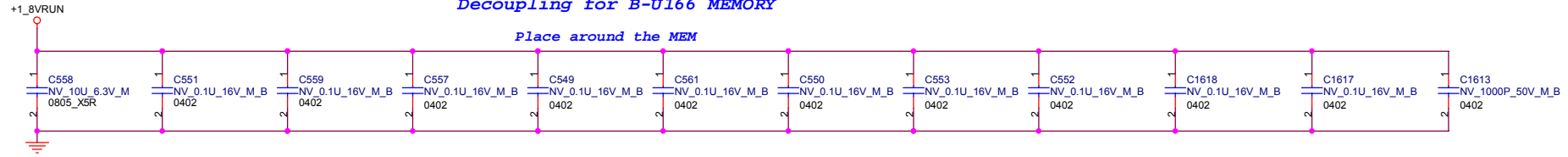
Decoupling for B-U165 MEMORY

Place around the MEM



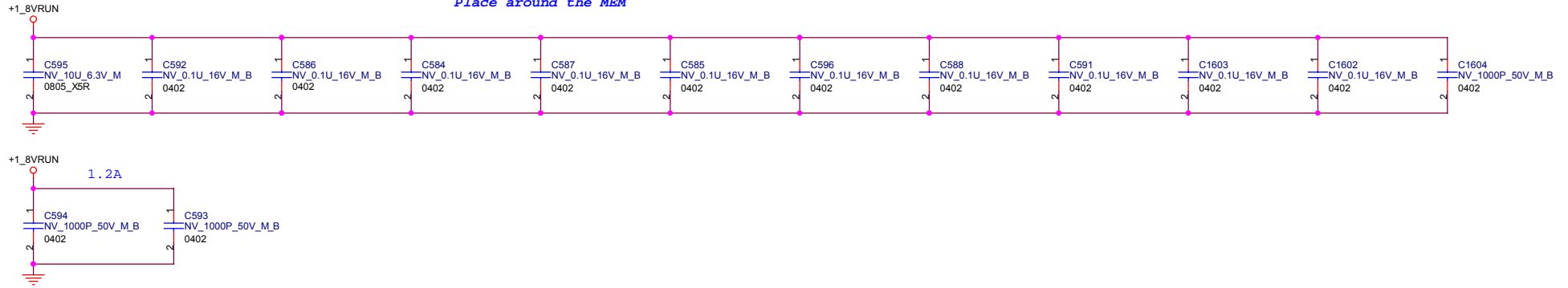
Decoupling for B-U166 MEMORY

Place around the MEM



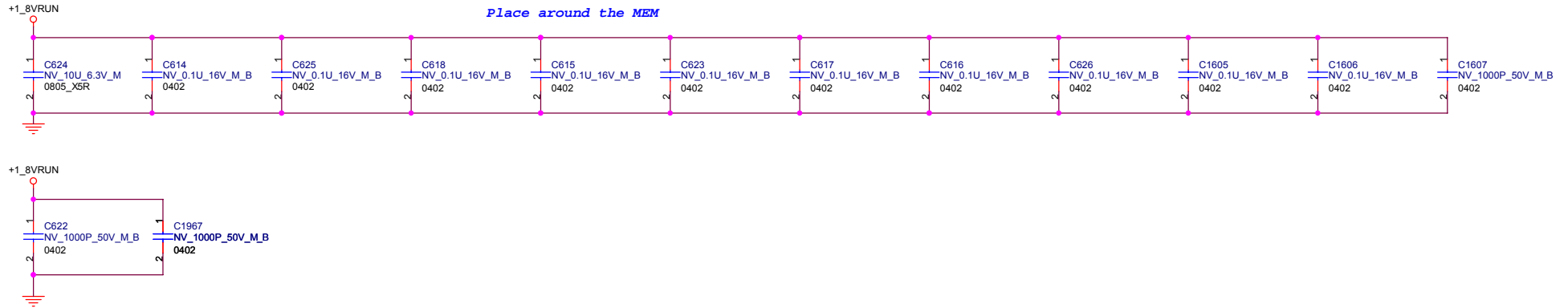
Decoupling for B-U167 MEMORY

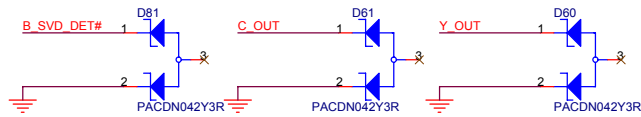
Place around the MEM



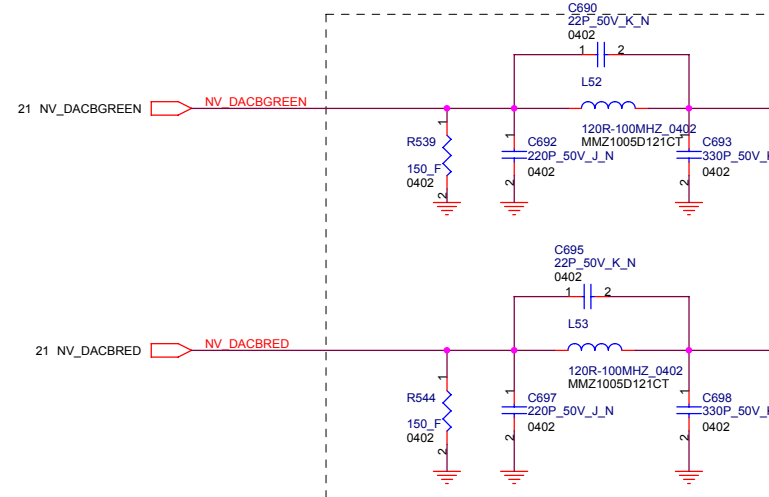
Decoupling for B-U168 MEMORY

Place around the MEM

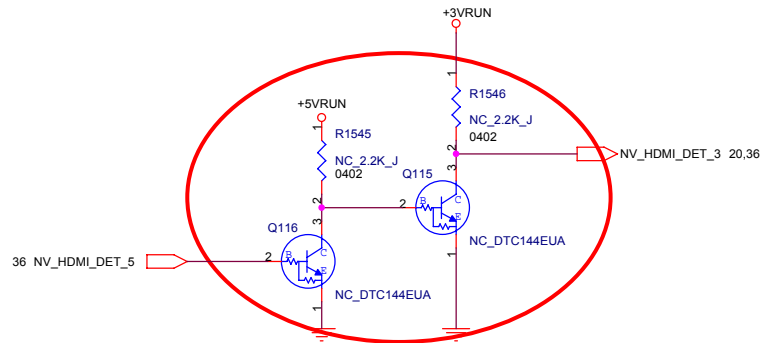
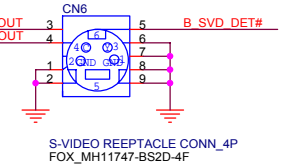




These component close to S-Video connector within 700 mil

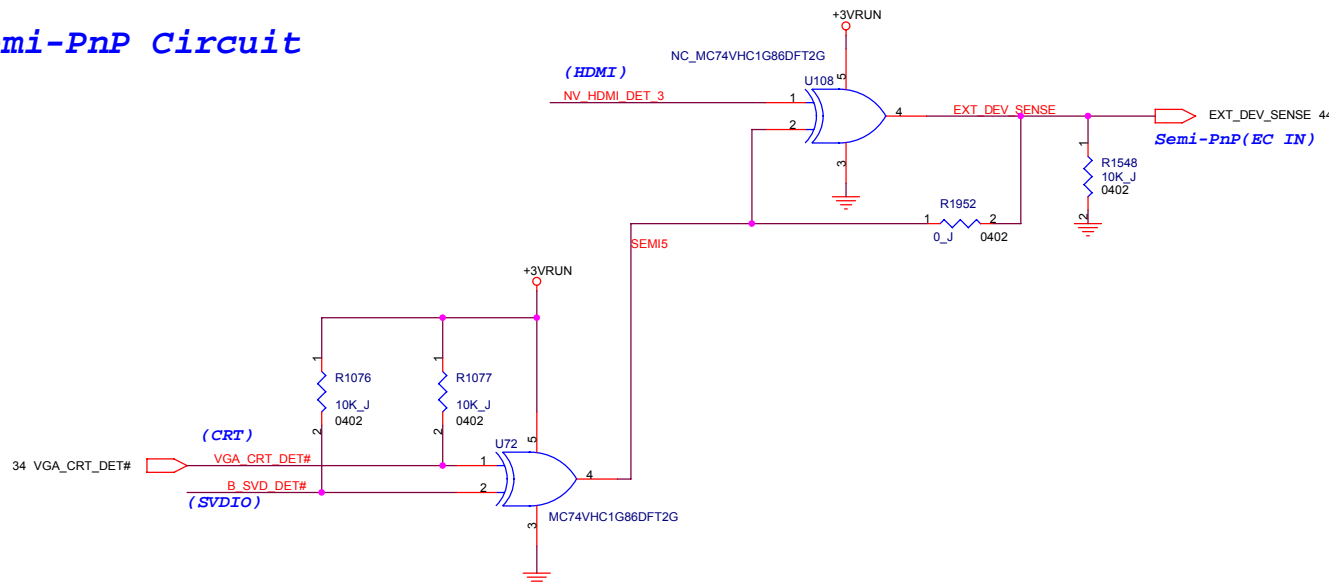


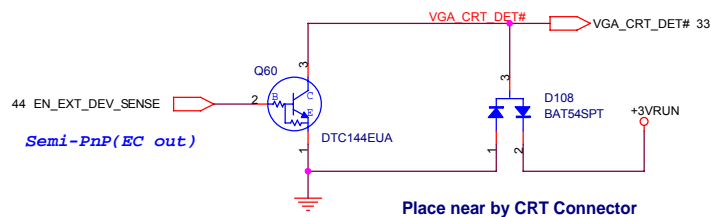
S-VIDEO CONNECTOR



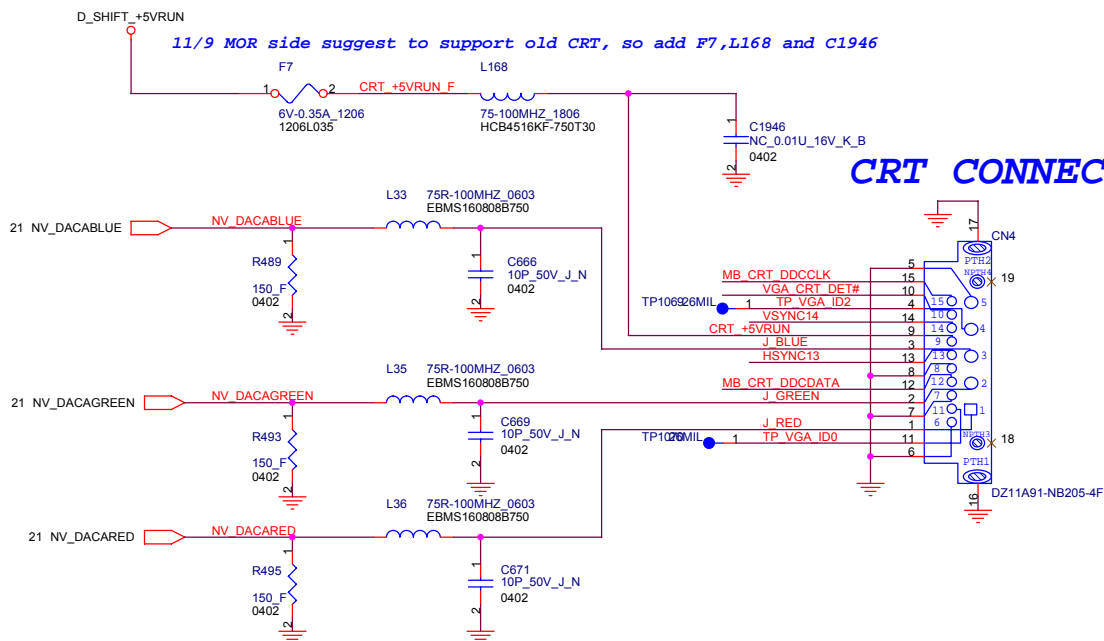
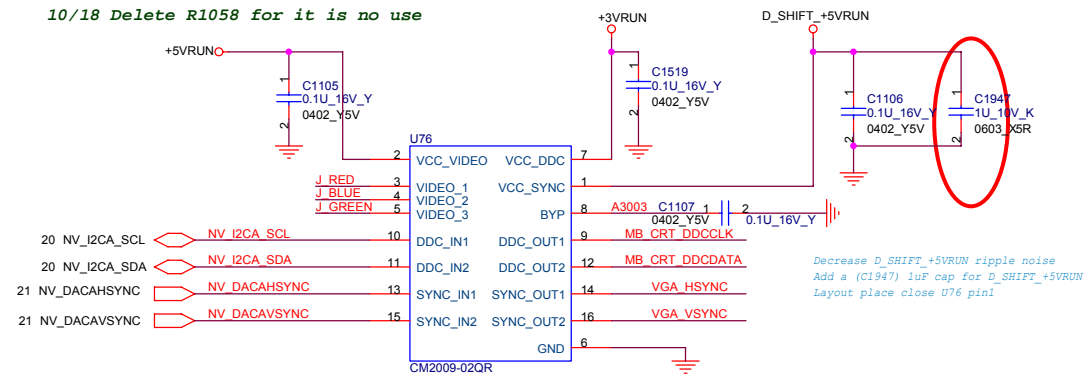
PS101 HPD has level shift function, so backup this circuit
Change Q115, Q116, R1545, R1546 to NC

Semi-PnP Circuit

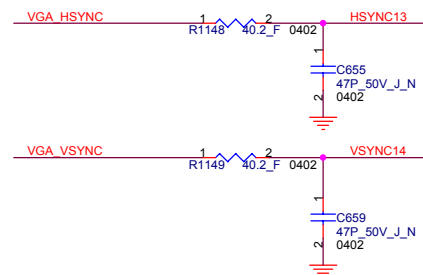




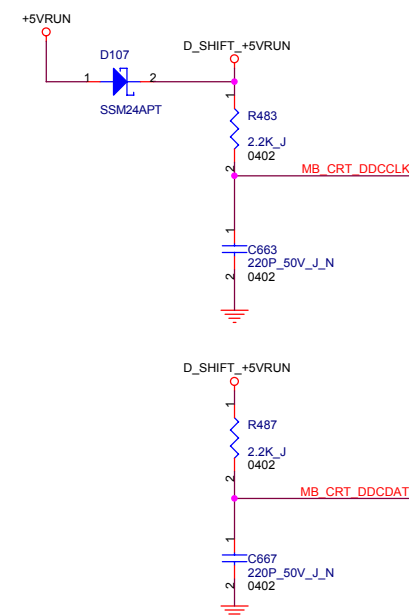
10/18 Delete R1058 for it is no use



CRT CONNECTOR

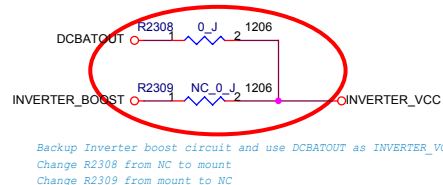
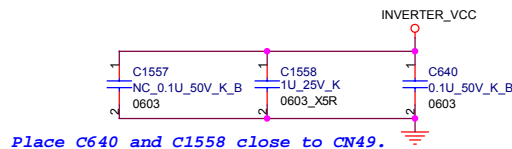


11/8 Change R1148, R1149 from 0ohm to 40ohm for meet CM2009-02 termination Spec

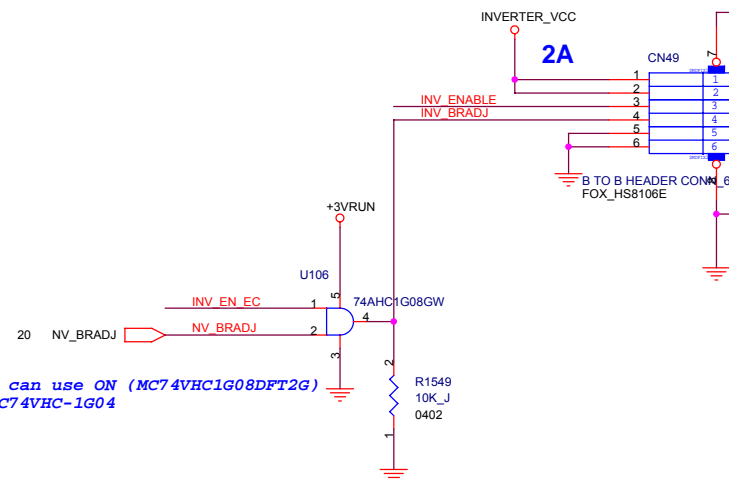


LVDS CONNECTOR

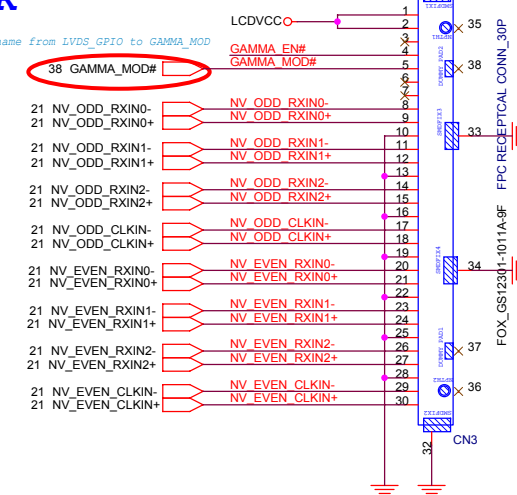
INVERTER CONNECTOR



U106,U15,U16 can use ON (MC74VHC1G08DFT2G)
H.H. PN:14-MC74VHC-1G04

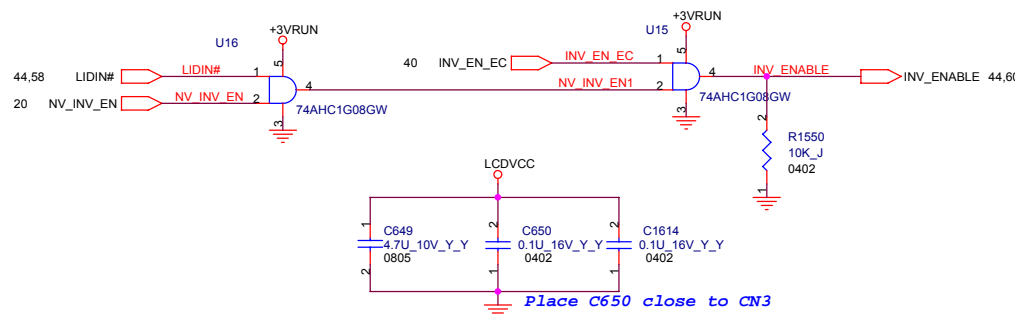


Change net name from LVDS_GPIO to GAMMA_MOD

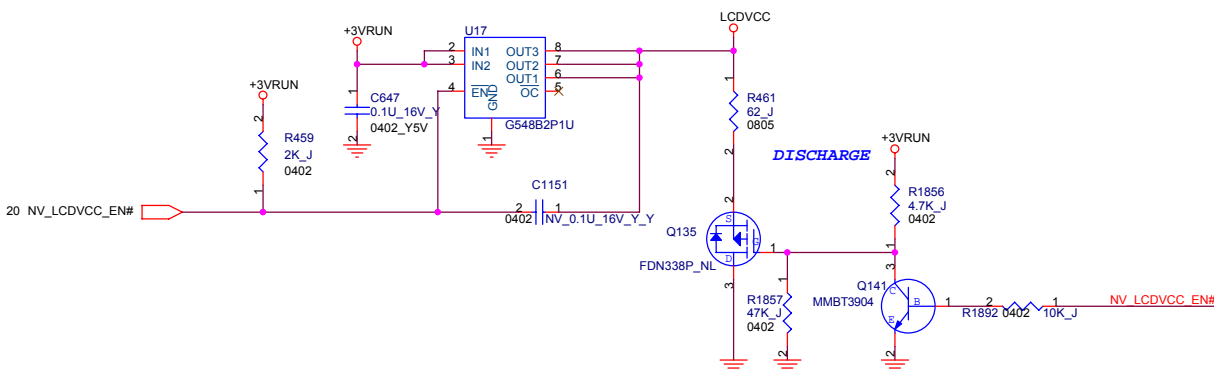


Use H/W selection to enable GAMMA function.
Change R1937,R1938 from 4.7K to 0ohm

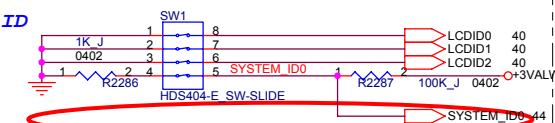
H: GAMMA Disable
L: GAMMA Enable



Current limit is from 1.1A to 2.1A.



PANEL ID



Type	WXGA+	WXGA+	WUXGA	WUXGA
Size	17" wide	17" wide	17" wide	17" wide
Vender	LG.PHILIPS	LG.PHILIPS	SHARP	SHARP
Device Name	LP171WP74-TLA1	LP171WP7-TLA1	LQ170M11LA4G	LQ170M11LA4B
Panel ID Check[2..0]	010	001	100	101

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title LVDS

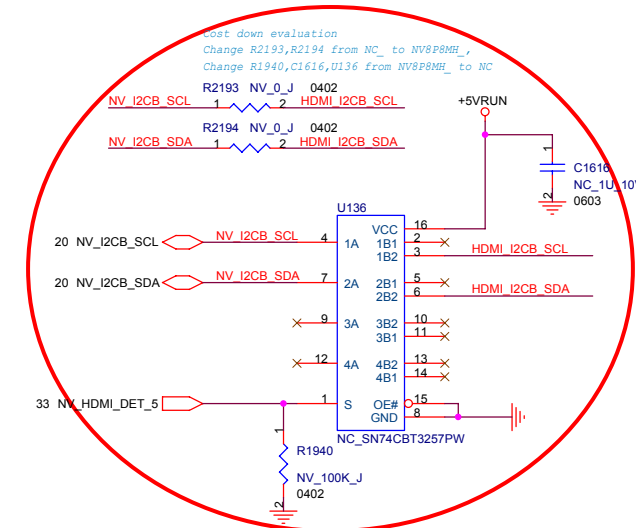
Size Document Number

Rev

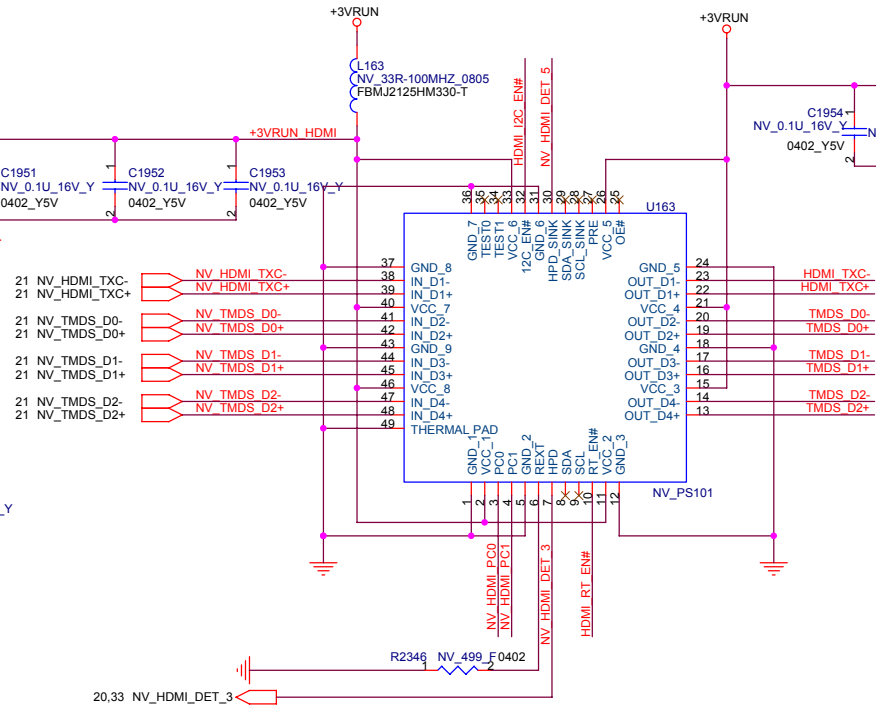
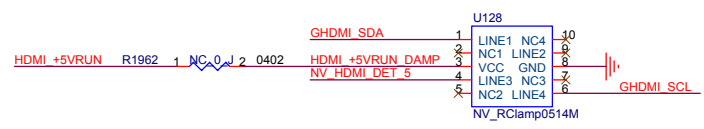
Date: Friday, August 31, 2007 Sheet 36 of 81

(TMDS inputs equalization control)
PC1,PC0 Configuration
00: 8 dB,
01: 4 dB,
10: 12 dB,
11: 0 dB

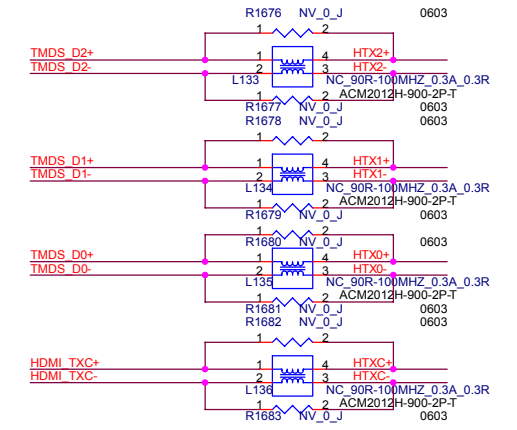
R2339 1 NV_10K 0402 NV HDMI PC0 R2340 1 NC_10K 0402
R2341 1 NC_10K 0402 NV HDMI PC1 R2342 1 NV_10K 0402
R2343 1 NC_10K 0402 HDMI RT_EN# R2344 1 NV_10K 0402
R2358 1 NV_10K 0402 HDMI I2C_EN#



HDMI DDC capacitance to GND need less than 50pF,so those parts need close to HDMI connector

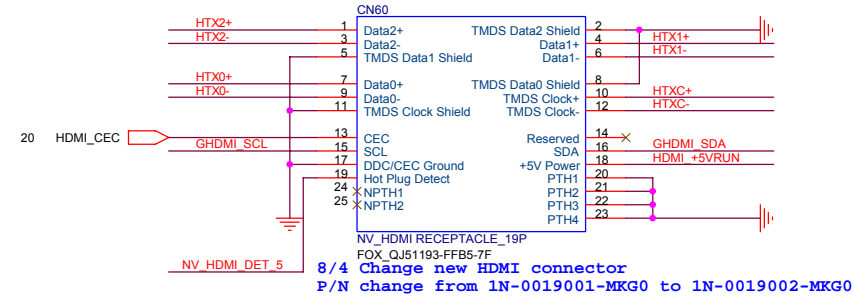


Add HDMI equalizer for M610 long trace issue

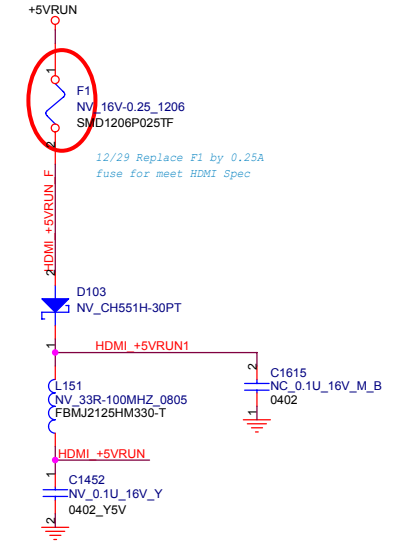
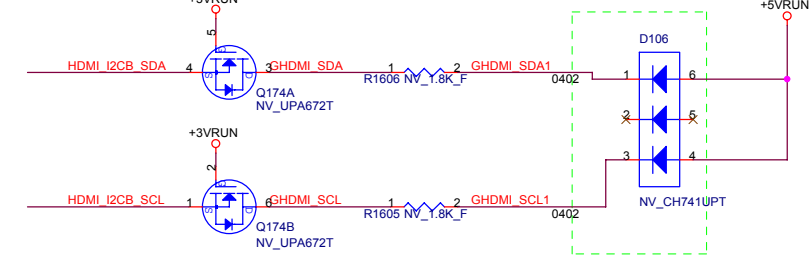


Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

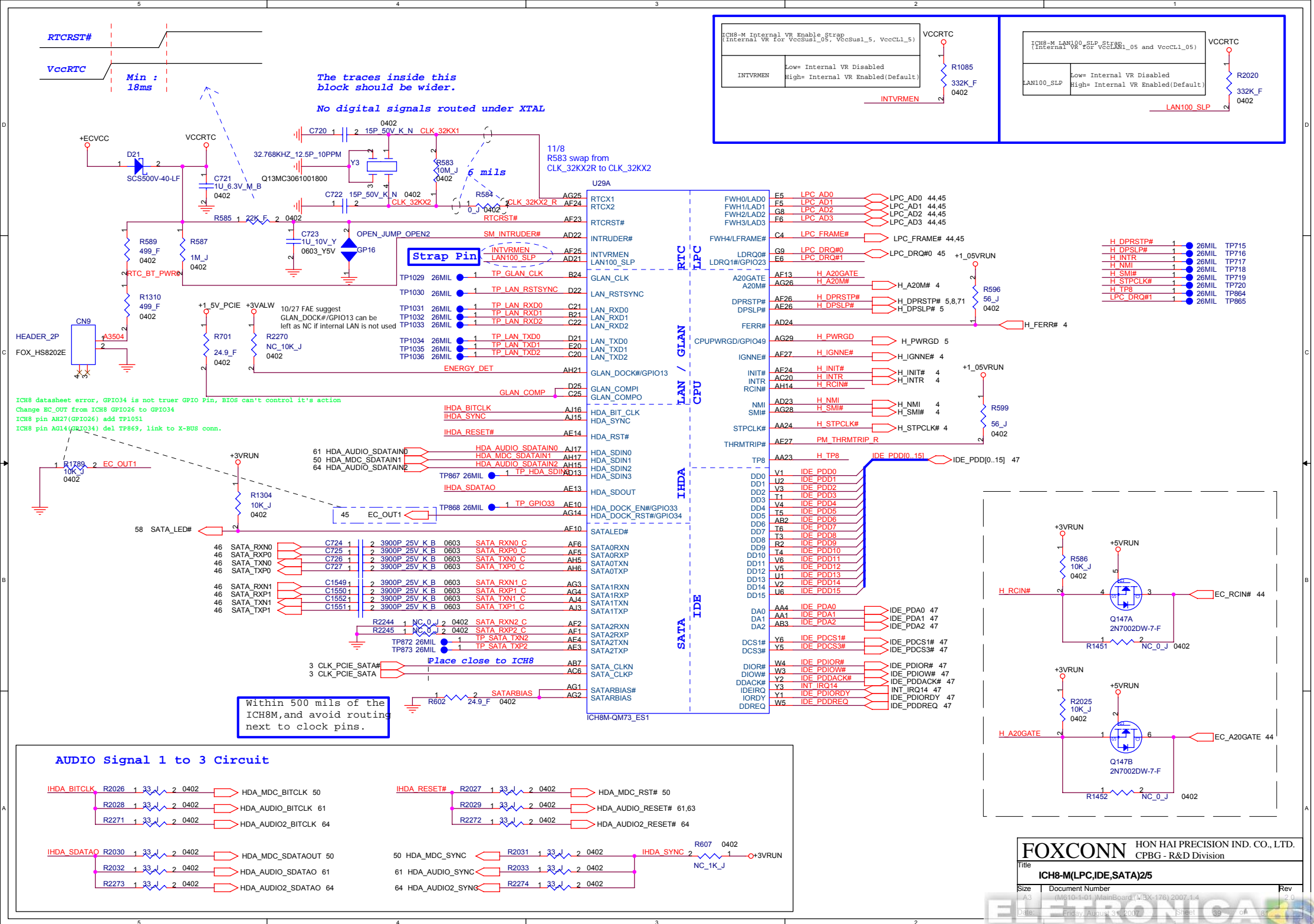
HDMI CONNECTOR

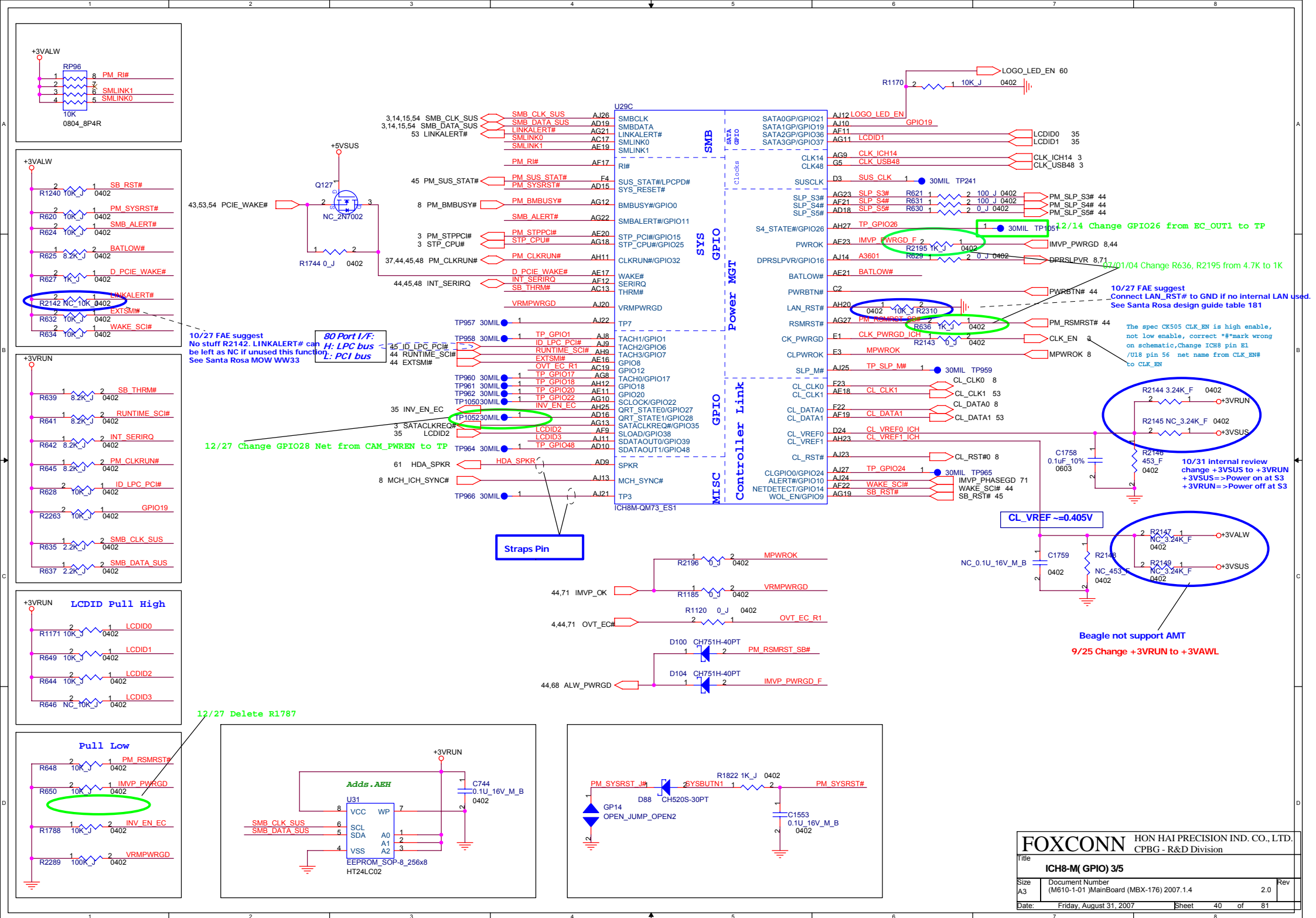


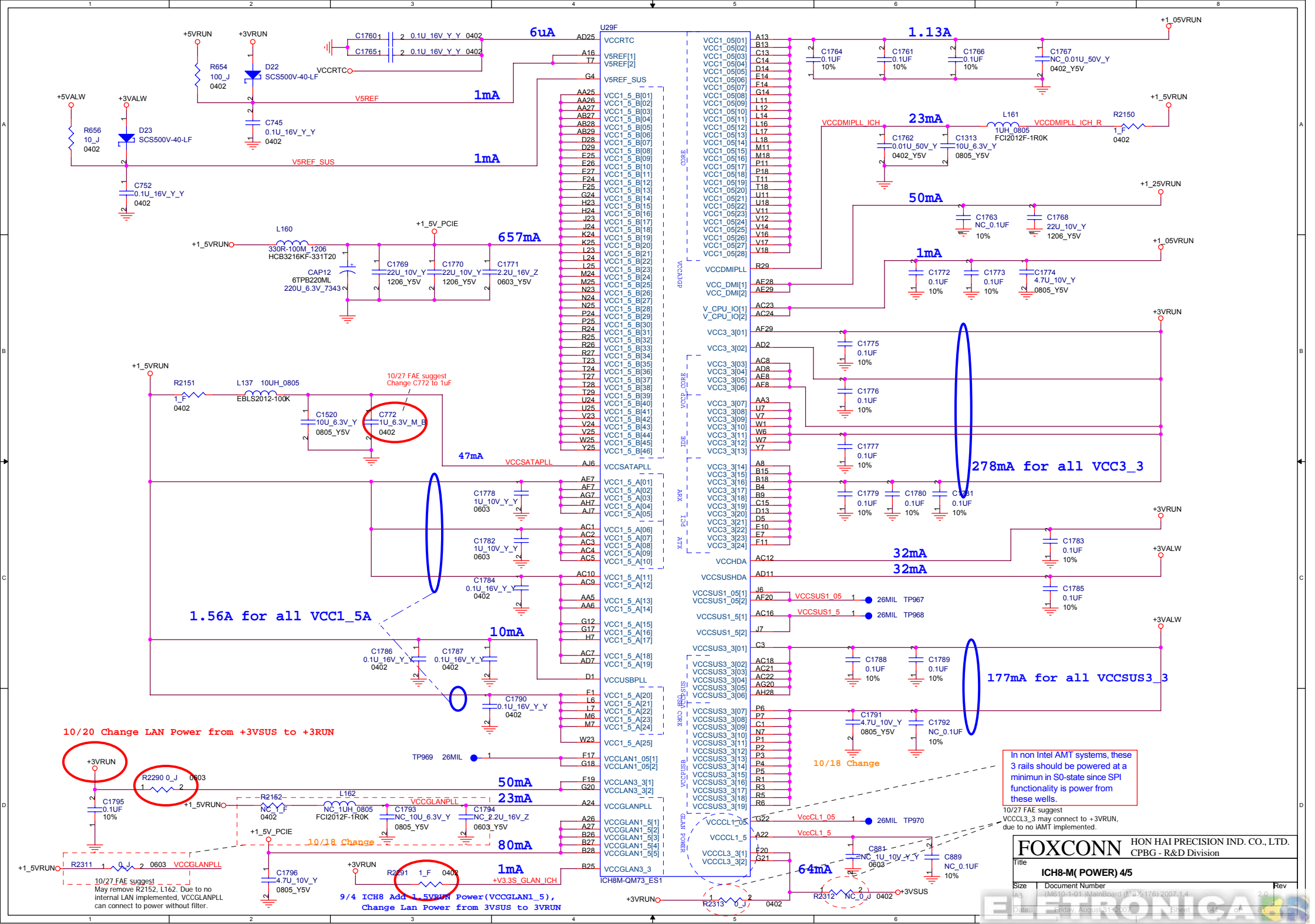
PVT Change to 16-CH741UP-T000

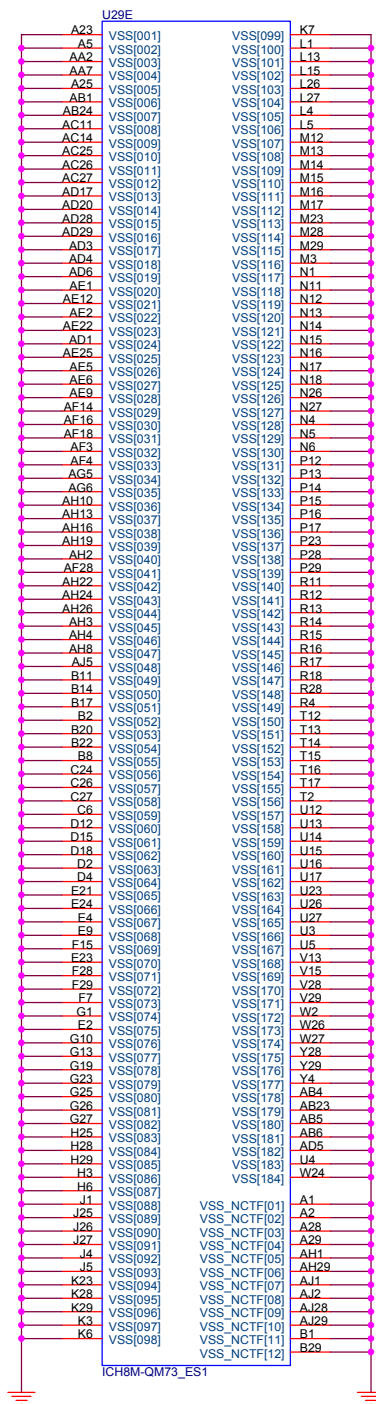


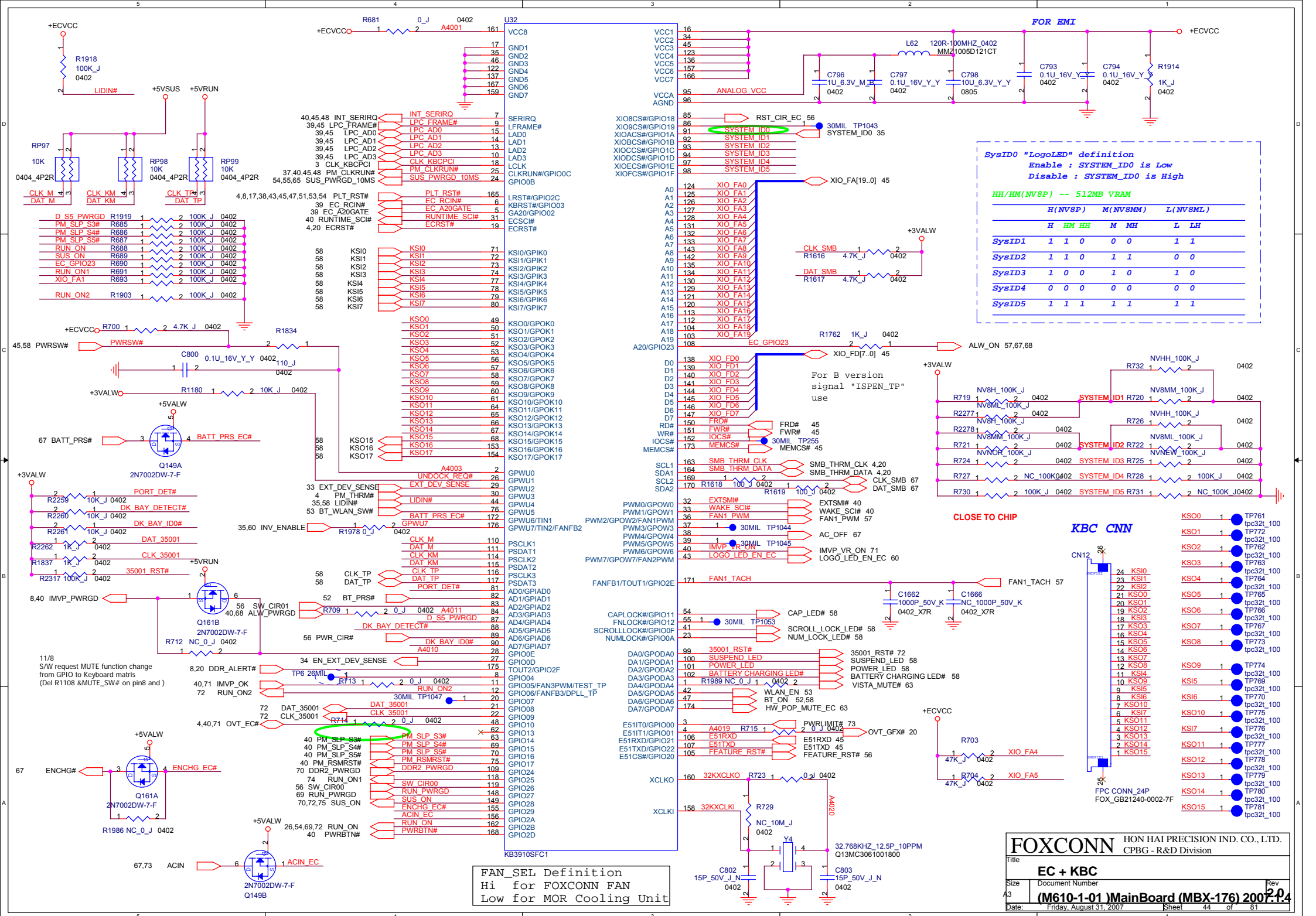
FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title	HDMI		
Size	Document Number	Rev	
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4	2.0	
Date:	Friday, August 31, 2007	Sheet	36 of 81











SysID0 "LogoLED" definition
Enable : SYSTEM_ID0 is Low
Disable : SYSTEM_ID0 is High

HH/HM(NV8P) -- 512MB VRAM

	H(NV8P)	M(NV8MM)	L(NV8ML)
SysID1	1 1 0	0 0	1 1
SysID2	1 1 0	1 1	0 0
SysID3	1 0 0	1 0	1 0
SysID4	0 0 0	0 0	0 0
SysID5	1 1 1	1 1	1 1

CLOSE TO CHIP

KBC CNN

FAN_SEL Definition
Hi for FOXCONN FAN
Low for MOR Cooling Unit

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title
EC + KBC

Size
A3

Document Number
(M610-1-01) MainBoard (MBX-176) 2007.1.4

Date
Friday, August 31, 2007

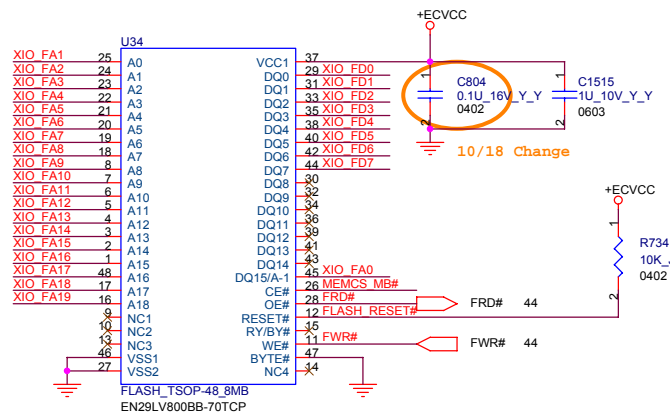
Sheet
44

of
81

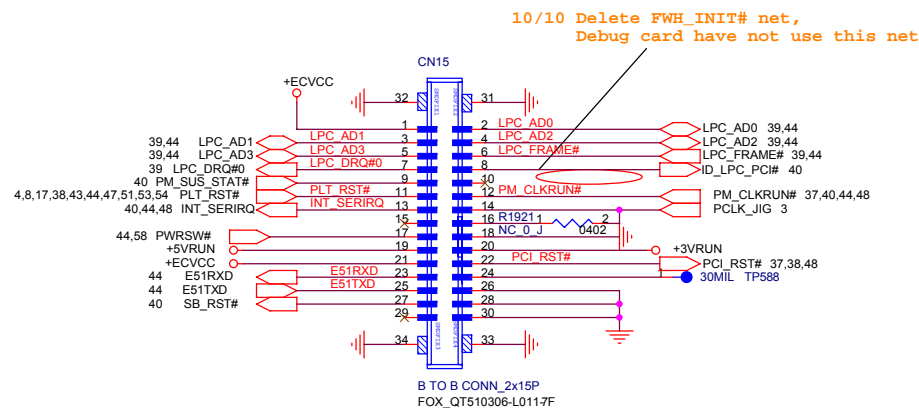
Rev
2.0

44 XIO_FA[19..0]
44 XIO_FD[7..0]

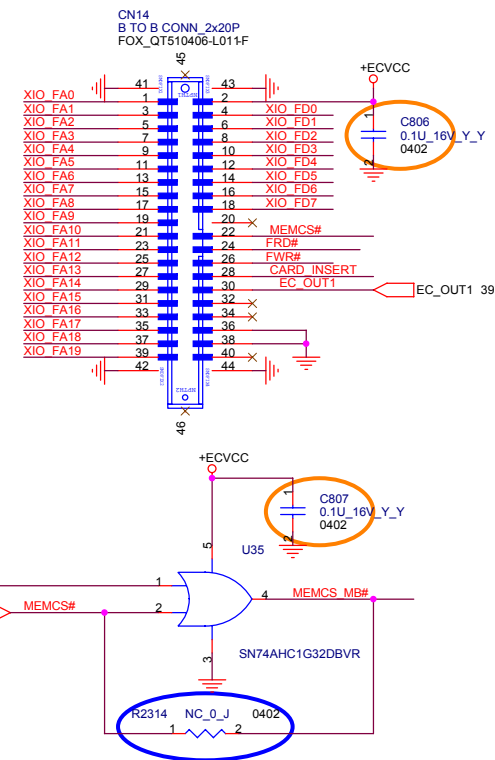
FLASH BIOS

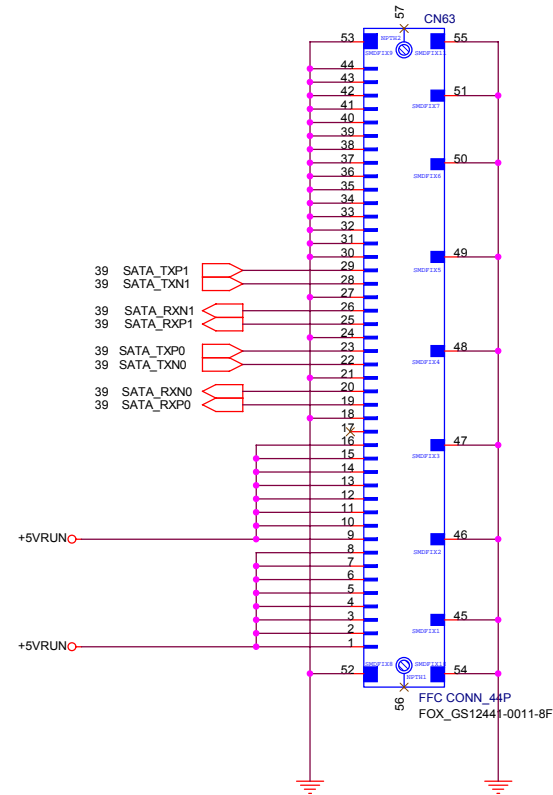
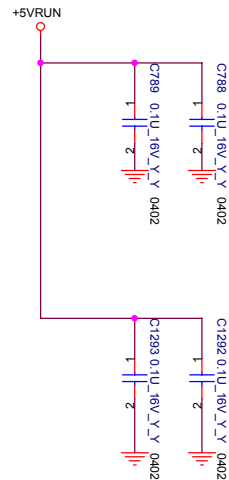


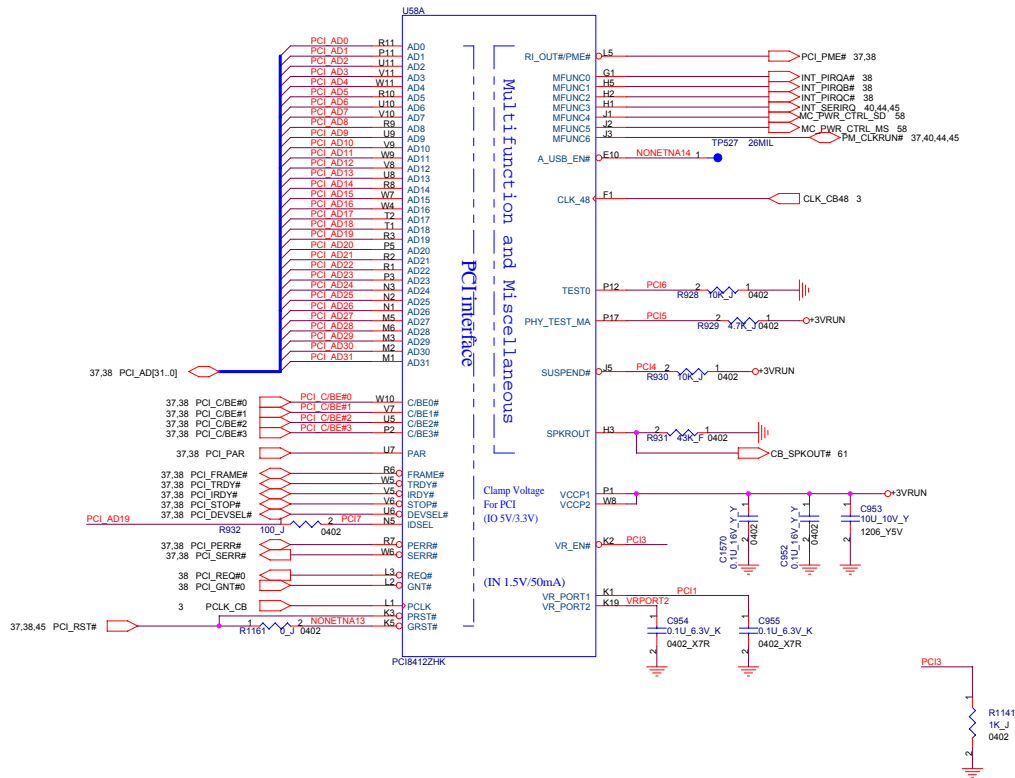
JIG-120



X-BUS

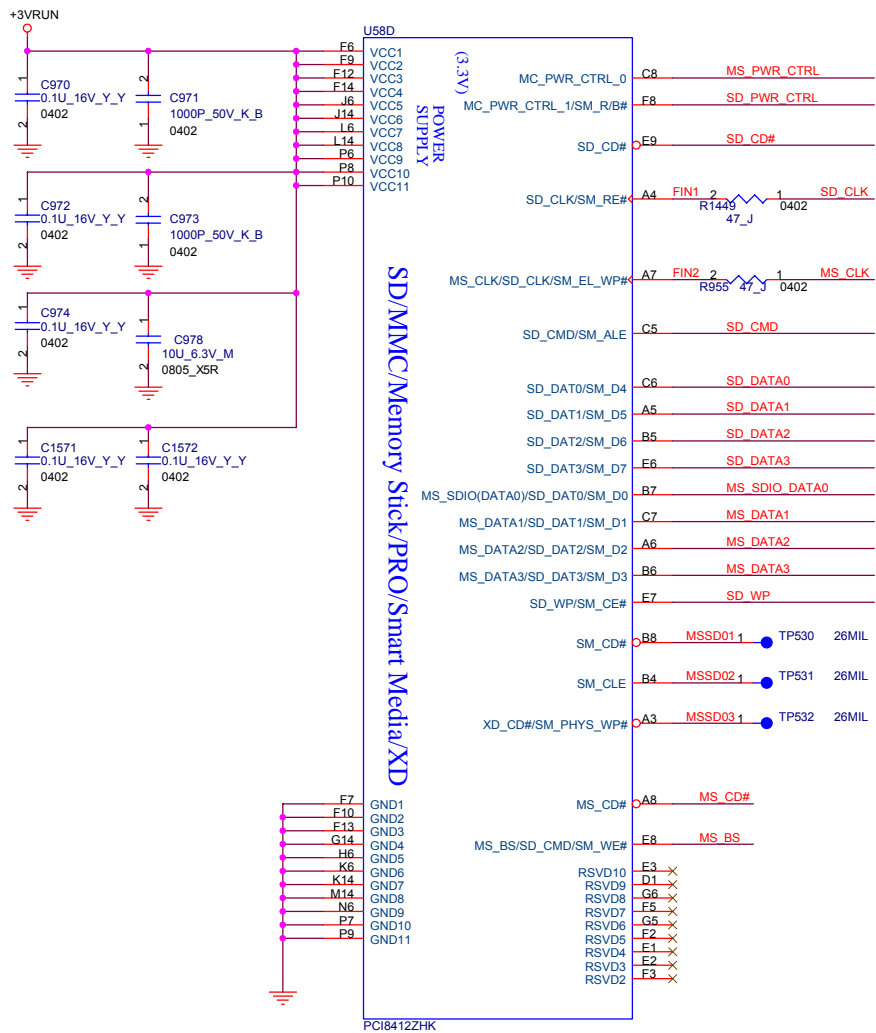




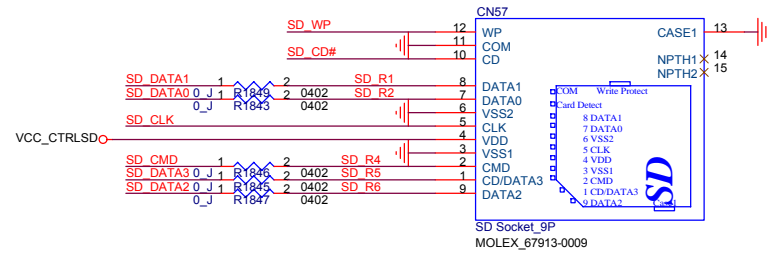


FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title PCI (PCI BUS)	
Size Custom	Document Number (MS10-1-01) MainBoard (MBX-176) 2007.1.4
Date: Friday, August 31, 2007	Rev 2.0
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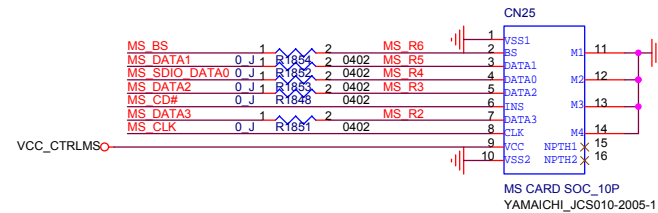




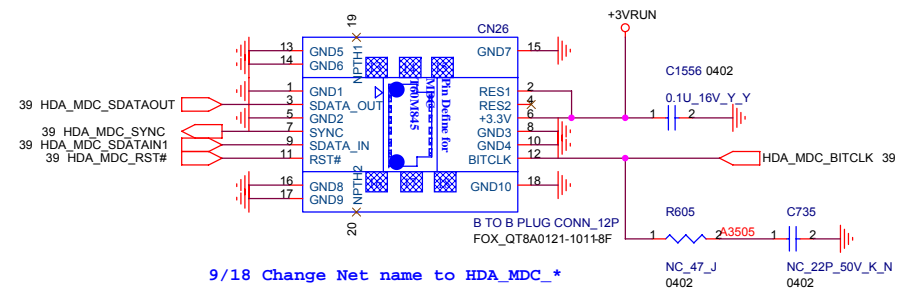
SD CONN.



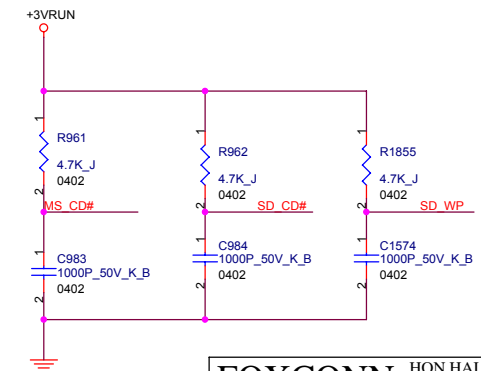
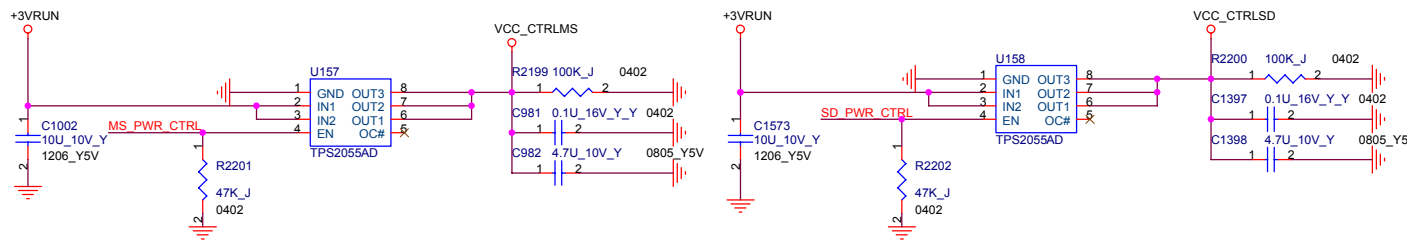
MS STD/DUO CONN.



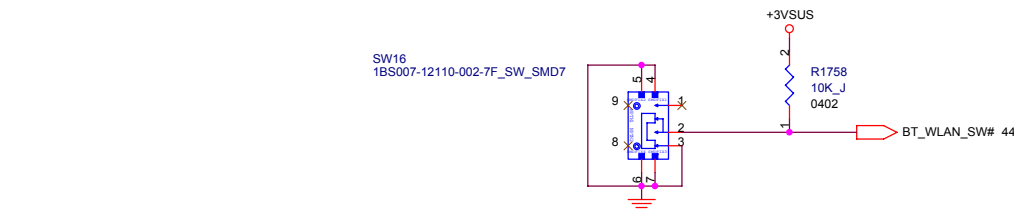
MDC CONN.



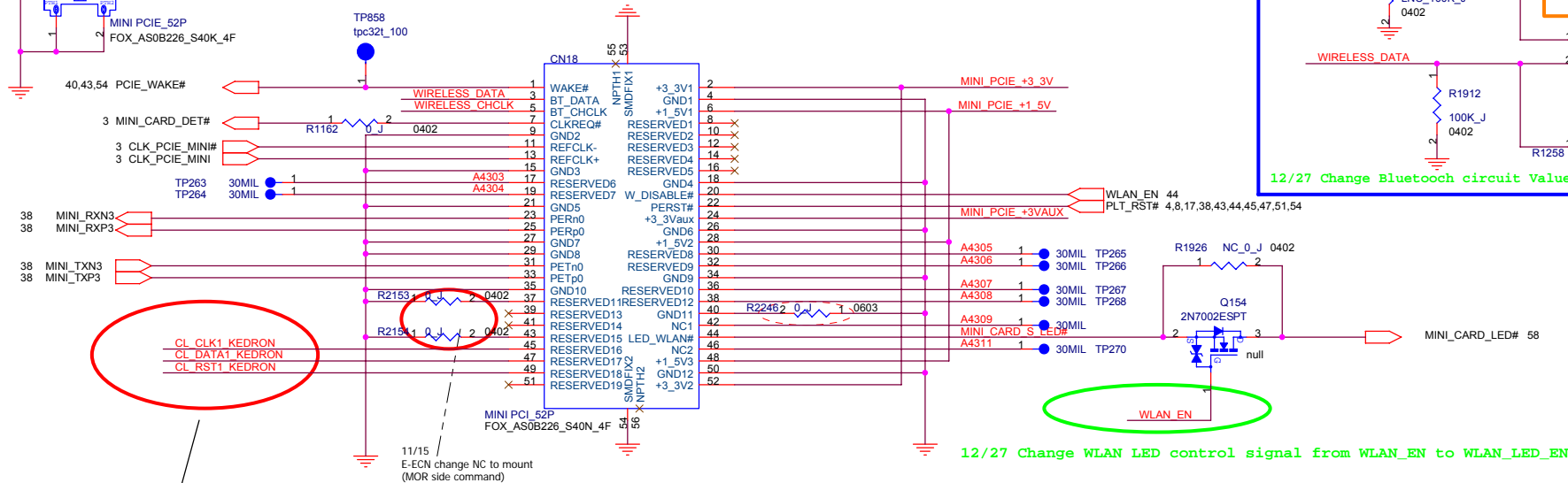
02/12/07 PVT Change MS Power switch to TPS2055



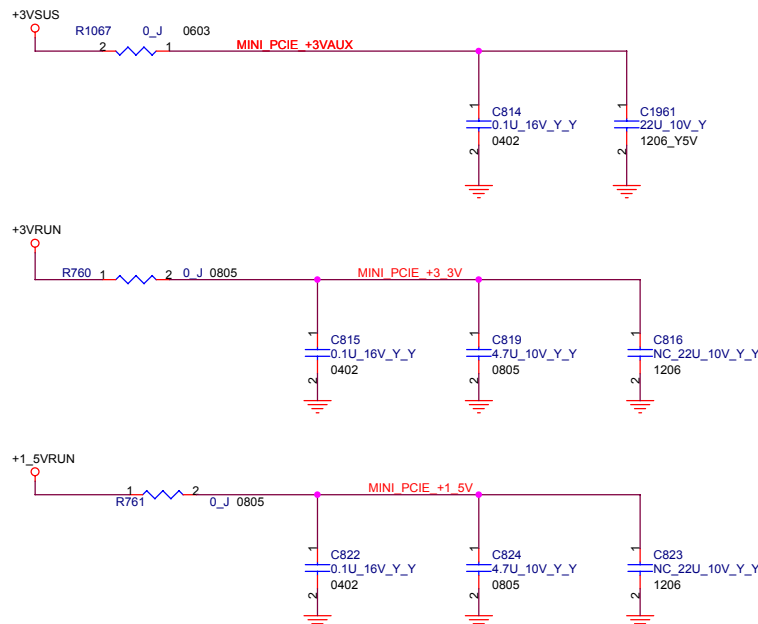
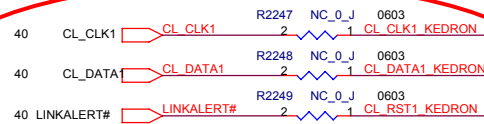
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
FAN/Bluetooth			
Size A3	Document Number (M610-1-01)MainBoard (MBX-176) 2007.14	2.0	Rev
Date:	Friday, August 31, 2007	Sheet	52 of 81



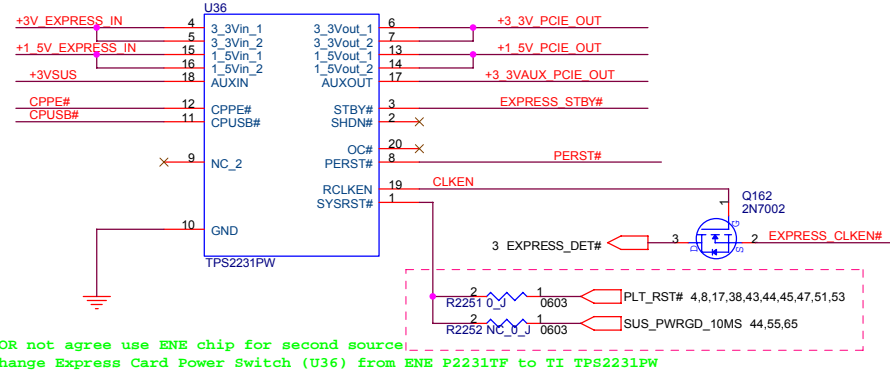
Mini-PCIE Card connector



10/27 FAE suggest
CL_CLK1/CL_DATA1/CL_VREF1 can be left as NC if unused iAMT. Don't need to connect to WLAN card.

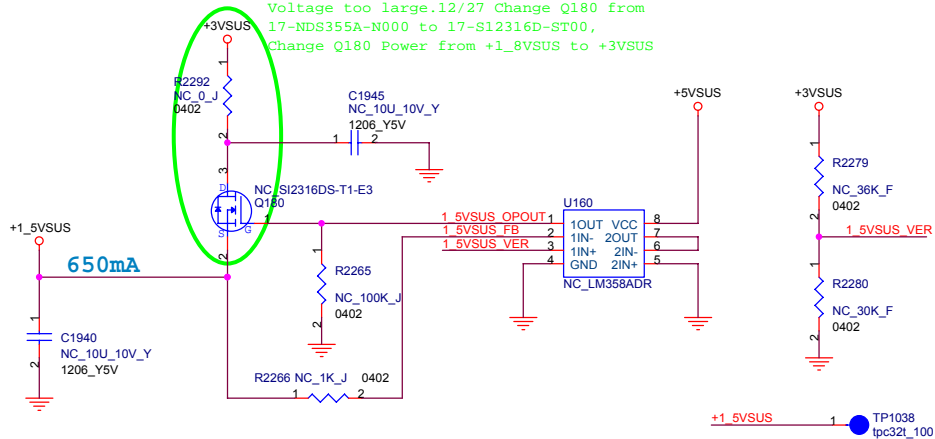


VOLTAGE INPUTS ⁽¹⁾			LOGIC INPUTS			VOLTAGE OUTPUTS ⁽²⁾			MODE ⁽³⁾
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP ⁽⁴⁾	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

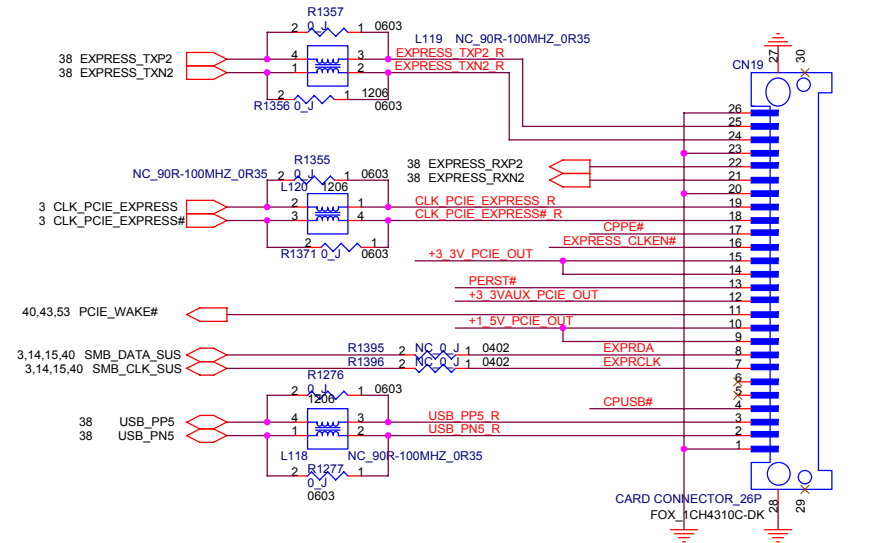


Constant-voltage +1_5VSUS

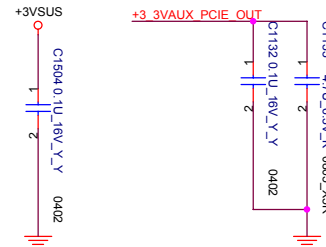
12/29 Load current test fial, 1.8V transfer 1.5V drop
Voltage too large.12/27 Change Q180 from
17-NDS355A-N000 to 17-SI2316D-ST00,
Change Q180 Power from +1_8VSUS to +3VSUS



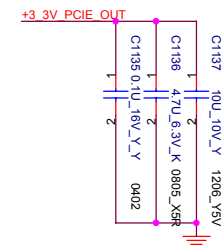
EXPRESS Card



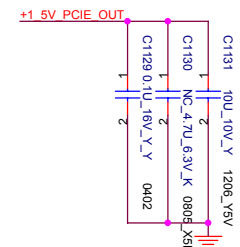
Supply Max 275mA



Supply Max 1300mA

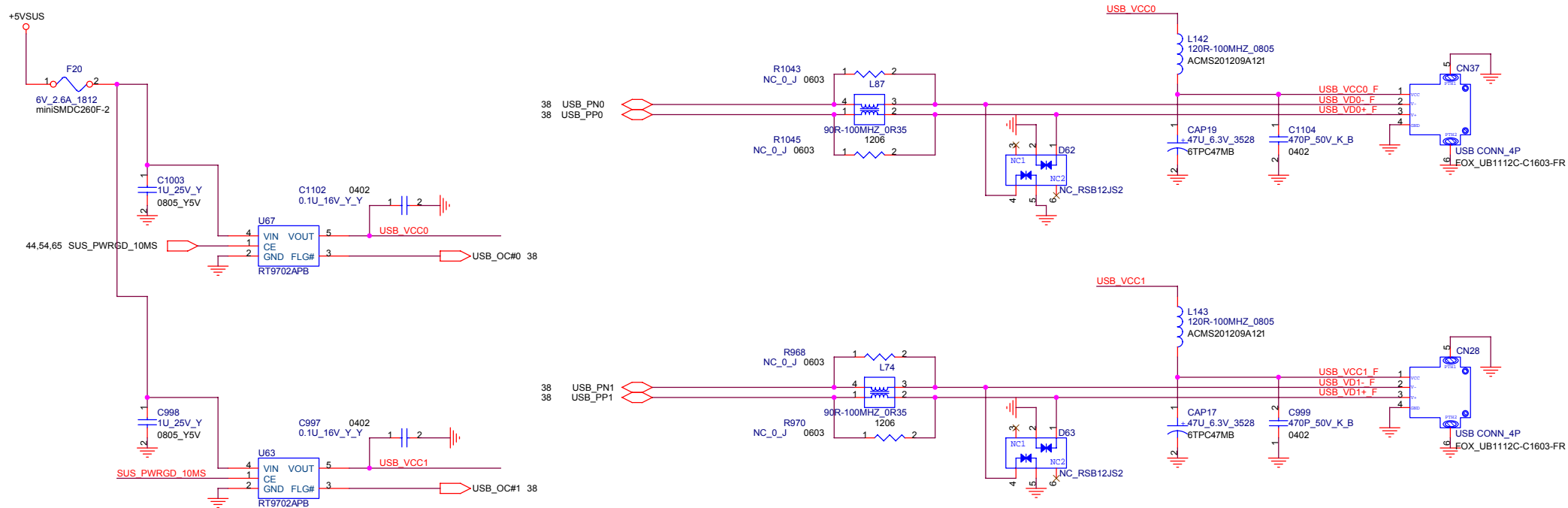


Supply Max 650mA

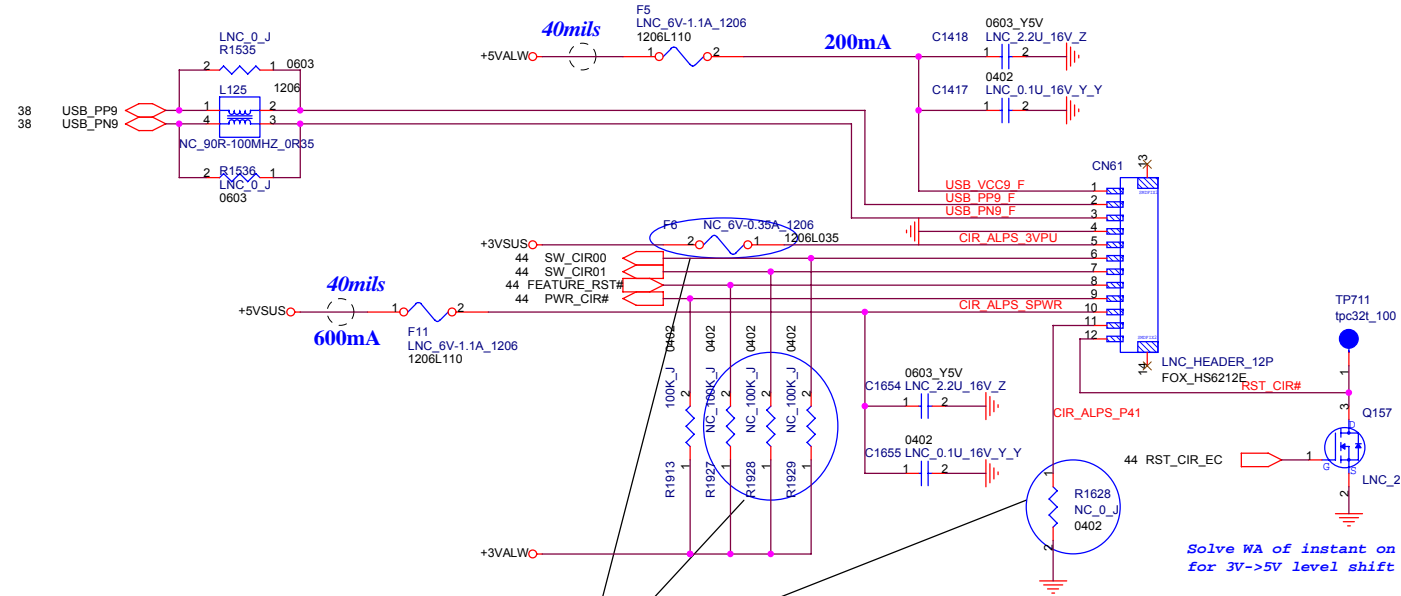


FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
EXPRESS CARD			
Size	Document Number	Rev	
A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0	
Date:	Friday, August 31, 2007	Sheet	54 of 81

USB connector *2



IR Rceiver connector



Button		SW1	SW0
VAIO button	Kick Instant On	L	L
Green button	Kick Windows	L	H
Shortcut button	Kick Windows	H	L
Standby button	Kick Windows	H	H

Num	Signal Name	I/O	Comment	Difference from ALPS.
1	+5VALW	VCC		<
2	USB+	I/O		<
3	USB-	I/O		<
4	GND	GND		<
5	+3VSUS	-	Not for use. Because SMK's IC use internal pull up resistor for D-.	ALPS's IC use this signal as a pull up plane of D- for low speed detection.
6	SW0	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
7	SW1	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
8	Feature_RST#	I	Software reset signal. (3.3V internal pull up resistor.)	Use for detecting of the remote button. 3.3V open drain output.
9	PWR#	O	Power on request signal. Open drain output.	<
10	SPWR	I	Power OK signal. 5V input.	<
11	EN	-	Not for use.	Low: Disable instant on feature Open or High: Enable instant on feature (3.3V internal pull up resistor.)
12	Hard_RST#	I	Hardware reset.	<

9/26 FOR NEW SMK IR module compatily
1.Change stuff to NC:F6,R1927,R1928,R1929,
2.EC Page GPIO20(105),GPIOAD2(83) pin swape

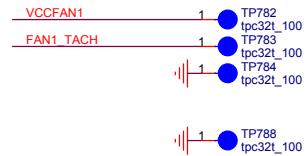
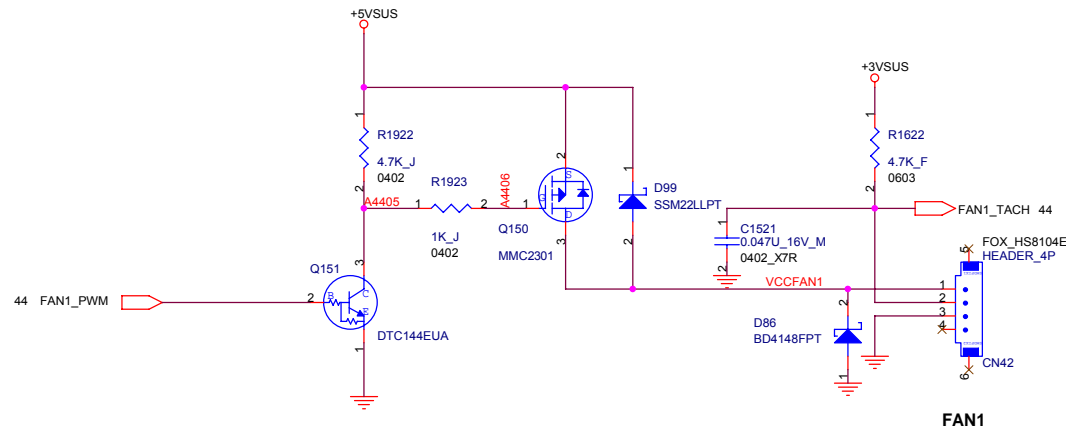
12/27 Change CIR circuit Value to LNC_* for M610 DVT L SKU

At Only USB Internal CIR, it's USB Power

USB_VCC9_F	1	TP847
USB_PP9_F	1	TP848
USB_PN9_F	1	TP849
	1	TP850
CIR_ALPS_3VPU	1	TP851
SW_CIR00	1	TP852
SW_CIR01	1	TP853
FEATURE_RST#	1	TP854
PWR_CIR#	1	TP855
CIR_ALPS_SPWR	1	TP856
	1	TP857

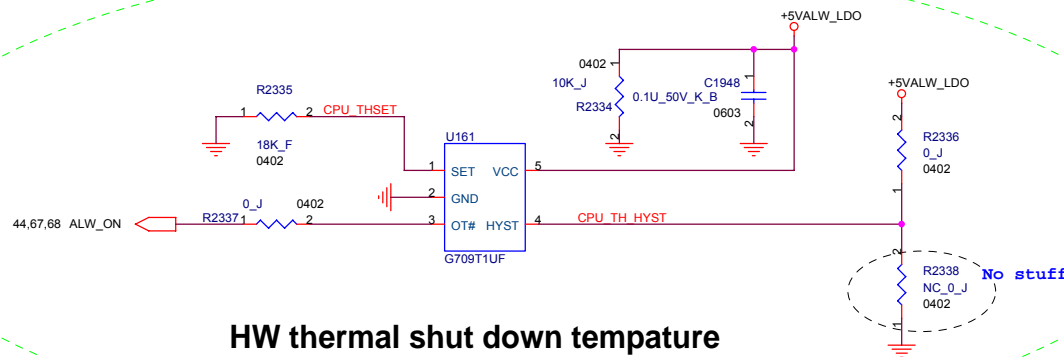
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
LED/LID SW#/Touch PAD			
Size	Document Number	Rev	
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4	2.0	
Date:	Friday, August 31, 2007	Sheet	56 of 81

FAN circuit



HW THERMAL PROTECTION

07/01/09 Change HW THERMAL PROTECTION circuit to stuff

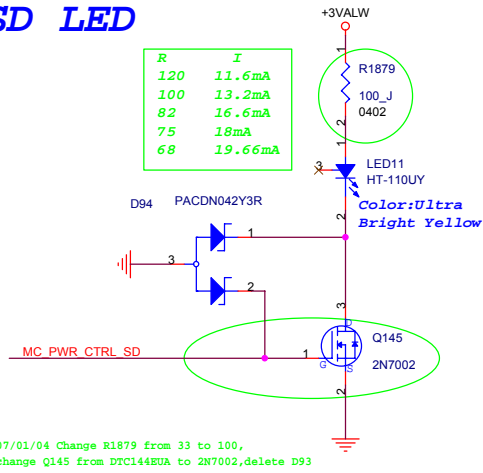


Base on MOR side request to add HW thermal protection circuit

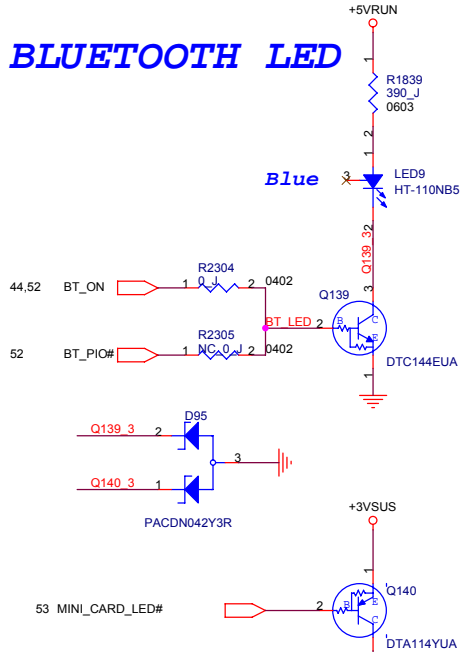
FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title			
FAN / HW THERMAL PROTECTION			

M610-1-01 MainBoard (MBX-176) 2007.12.0

SD LED

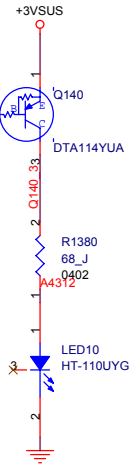


BLUETOOTH LED

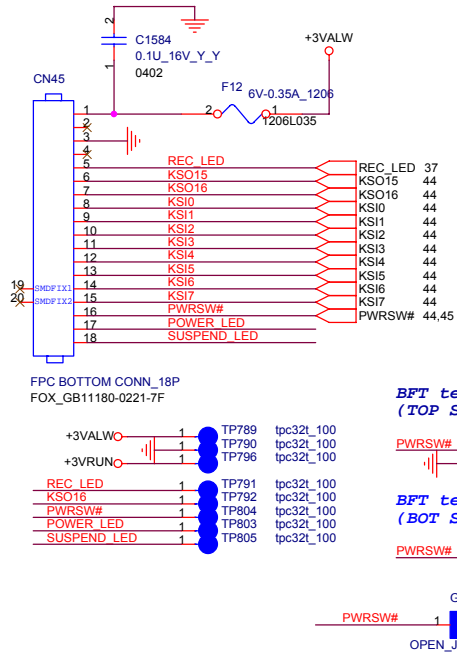


WLAN LED

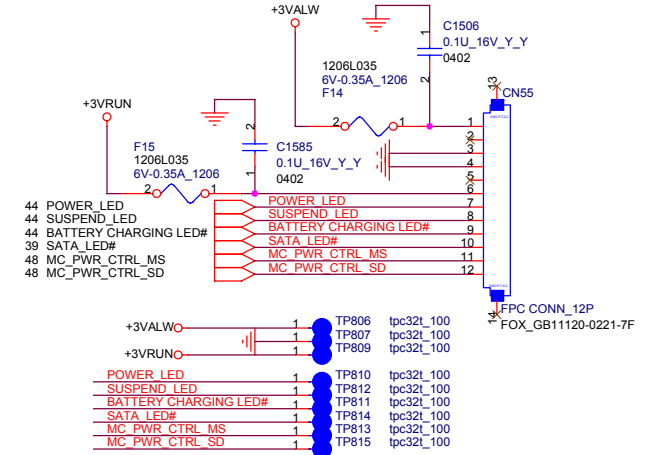
LED IF SPEC:
20mA(TYP), 30mA(MAX)



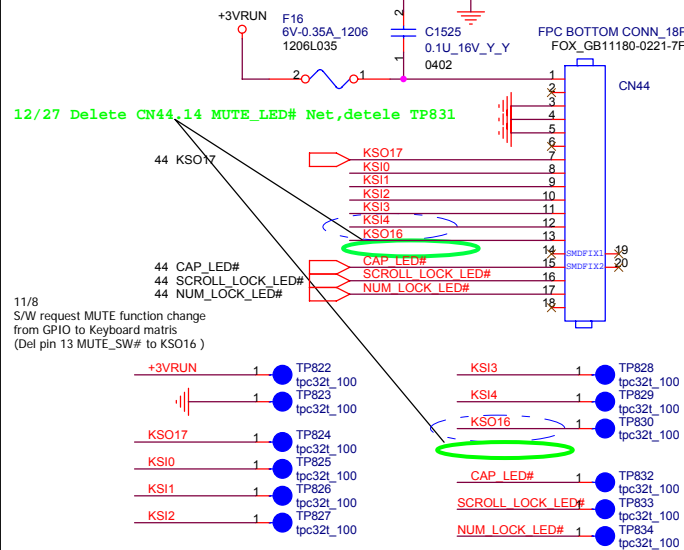
To Power Button Board Connector



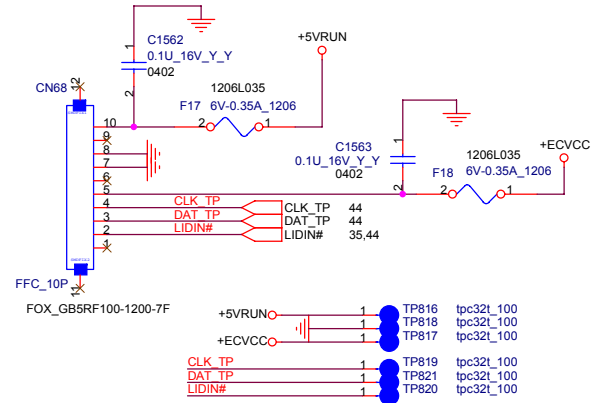
To LED Board Connector



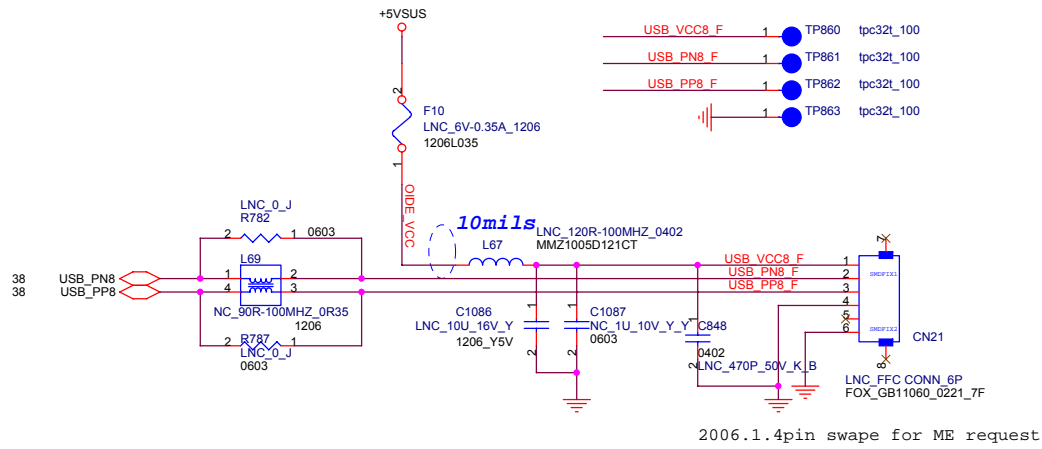
To AV Function Board Connector



To Touch Pad Board Connector

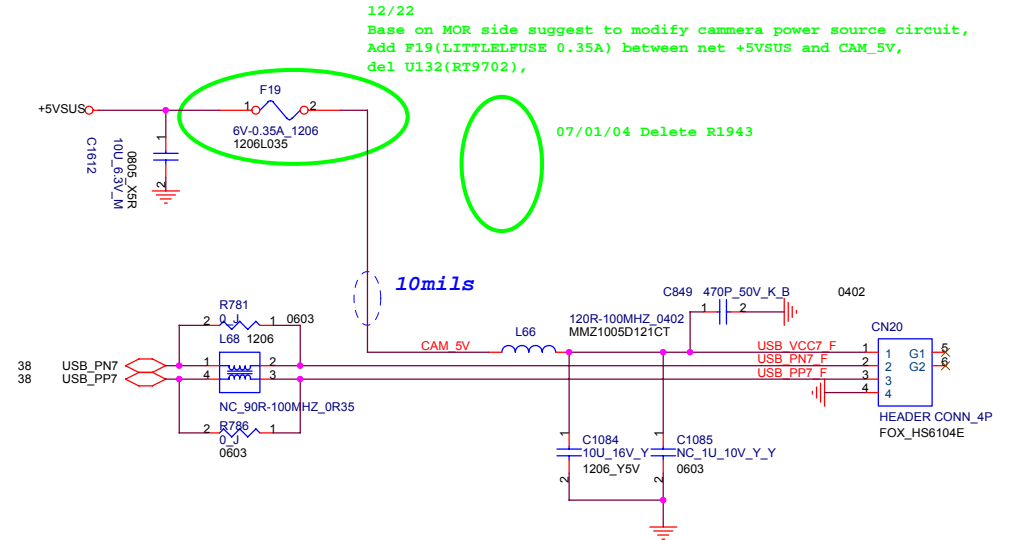


OIDE Connector

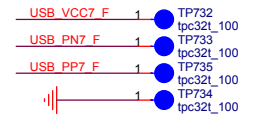


12/27 Change Felica circuit Value to LNC_* for M610 DVT I SKU

CAMERA Connector



12/21 BPT Test Pad



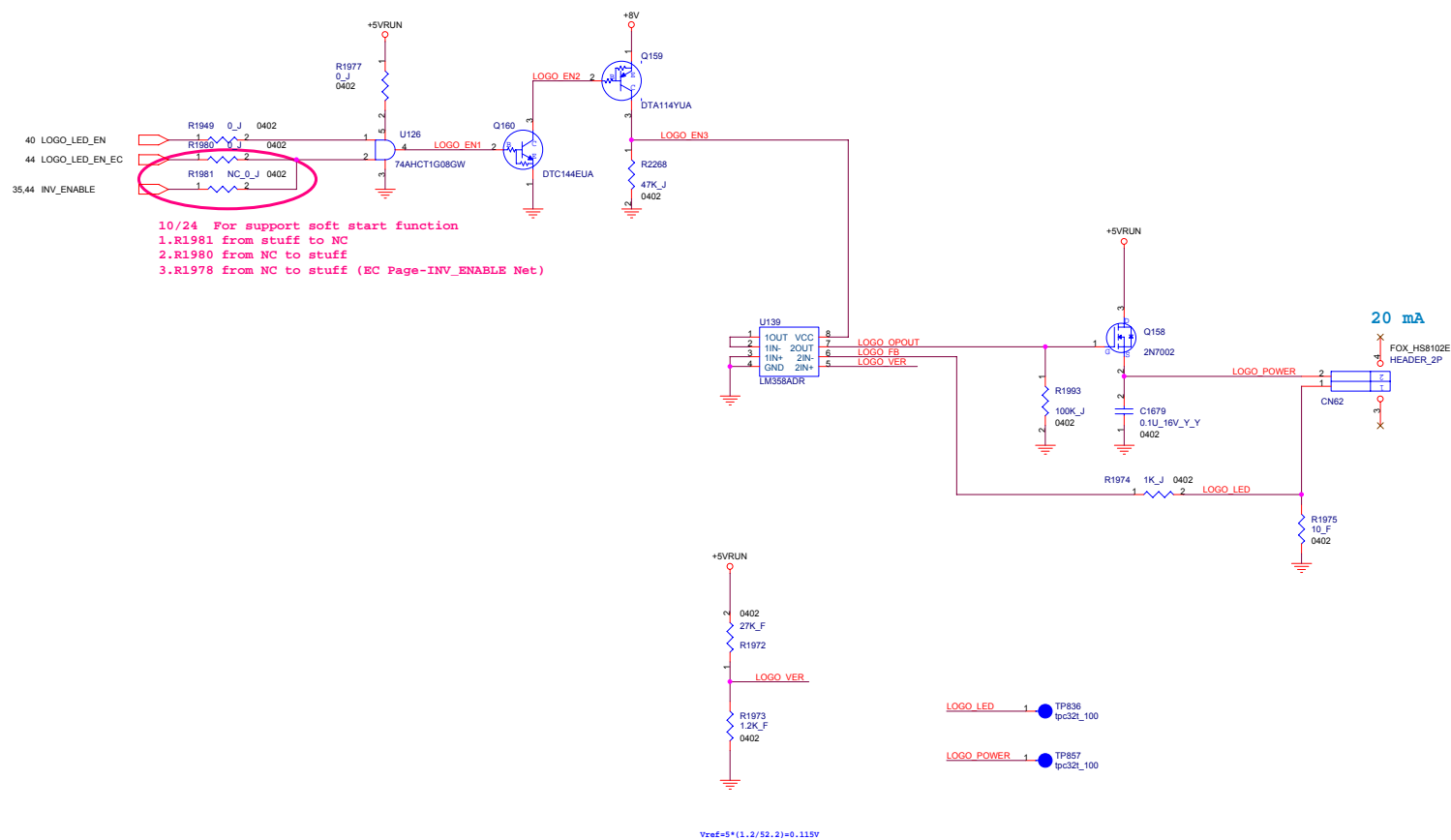
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title **CAM/OIDE**

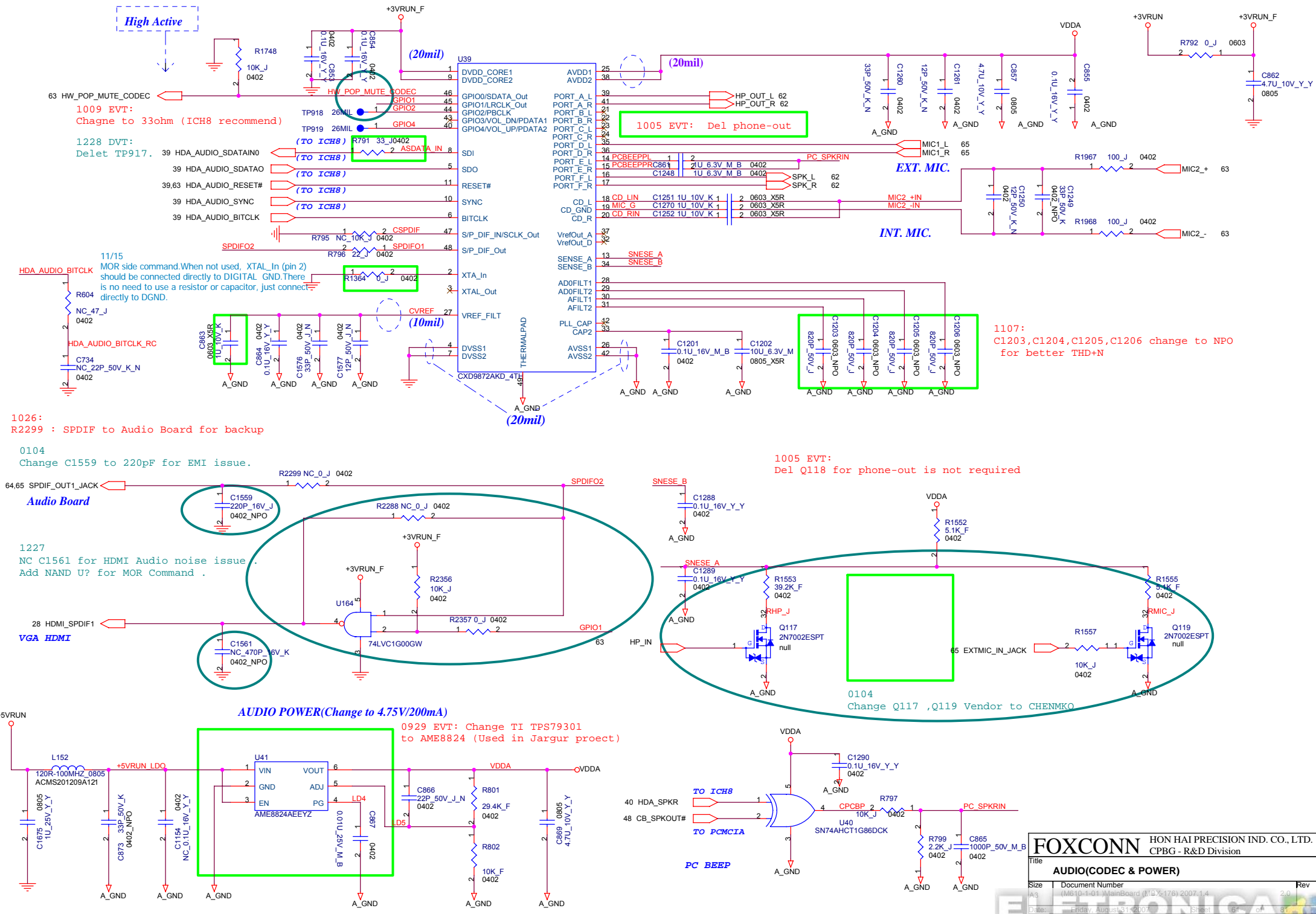
Size Document Number (M610-1-01) MainBoard (MRX-176) 2007 1.4 2.0 Rev

Date: Friday, August 31, 2007 1 Sheet 99 of 81

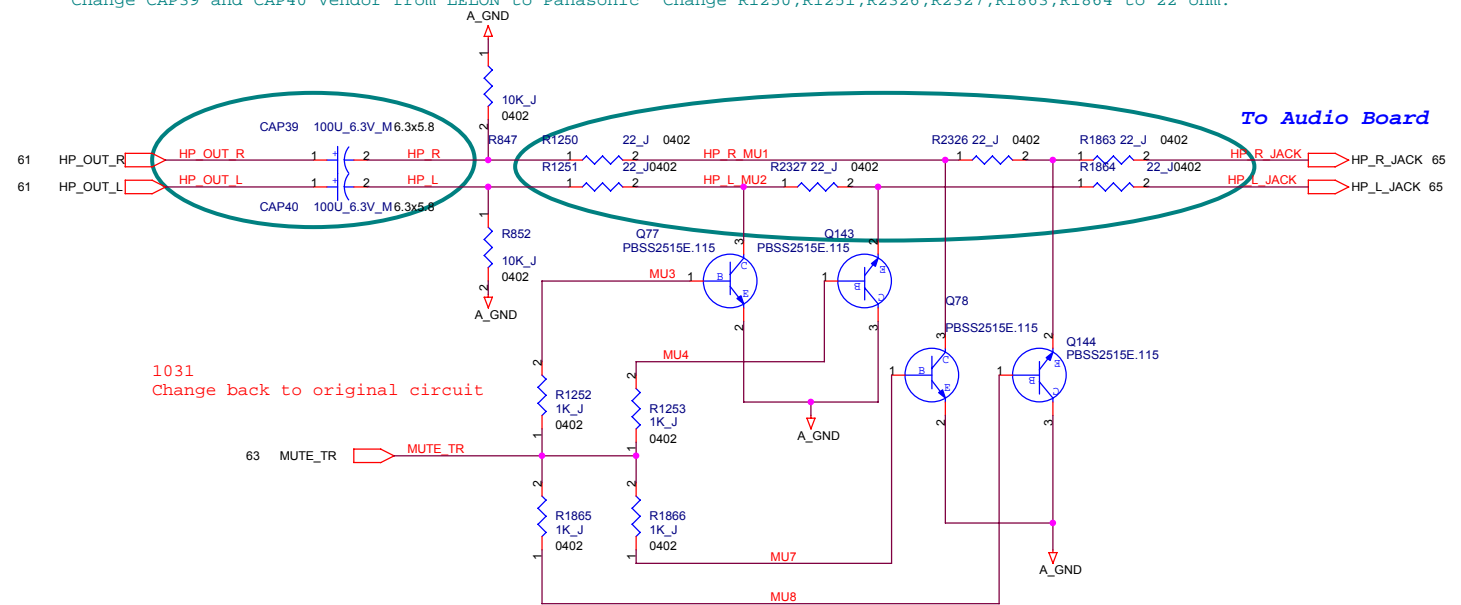
Constant-Current SONY LOGO LED



FOXCONN		HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title Logo LED / +1_5VSUS			
Size Custom	Document Number (M610-1-01) MainBoard (MBX-176) 2007.14		Rev 2.0
Date: Friday, August 31, 2007		Sheet 60 of 81	

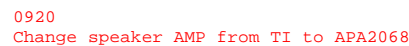


1228	1229
Change CAP39 and CAP40 Vendor from LELON to Panasonic	Change R1250,R1251,R2326,R2327,R1863,R1864 to 22 ohm.



63 MUTE_TR MUTE_TR

0920
Change to 0ohm 0603



Gain	R2216	Voltage
8dB	9.1K	0.77V
10dB	7.68K	0.65V
12dB	6.2K	0.54V
14dB	4.7K	0.43V
16dB	3.3K	0.31V

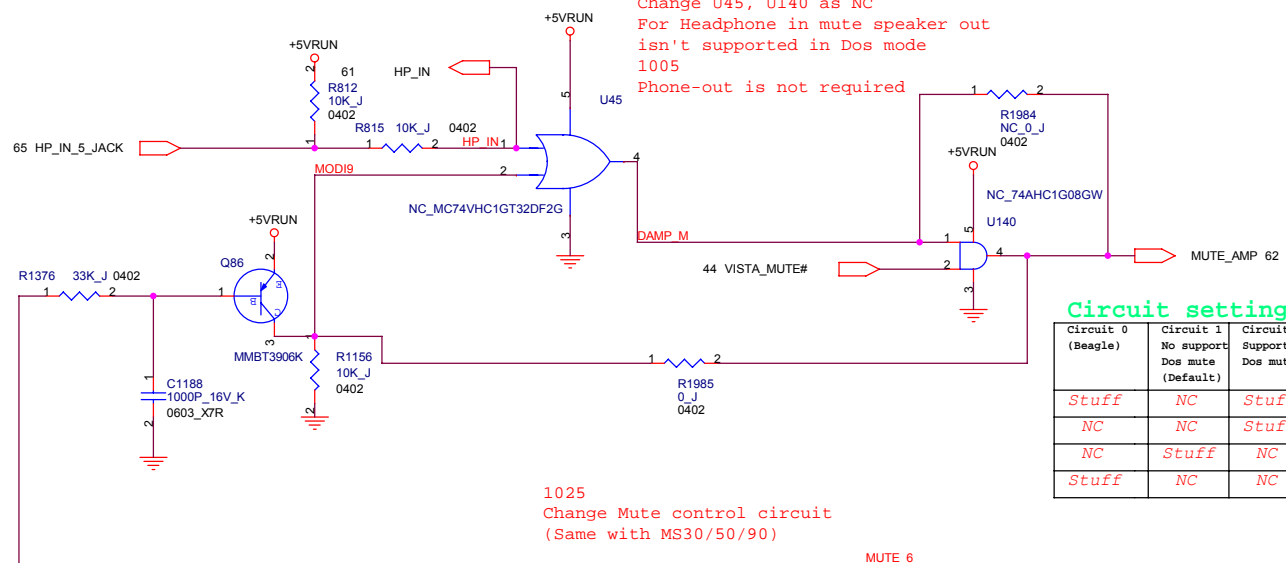
```
1209
Change gain setting to 14dB ,R2216 from 3.3K to 4.7K.
When play -3dB sine wave file ,the power is 1.2W.
```

Title	AUDIO(AMP & HP & SPK)
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Size	Document Number	Rev
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A3	(M610-1-01)MainBoard (MBX-176) 2007.1.4	2.0
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Date:	Friday, August 31, 2007	Sheet	62	of	81
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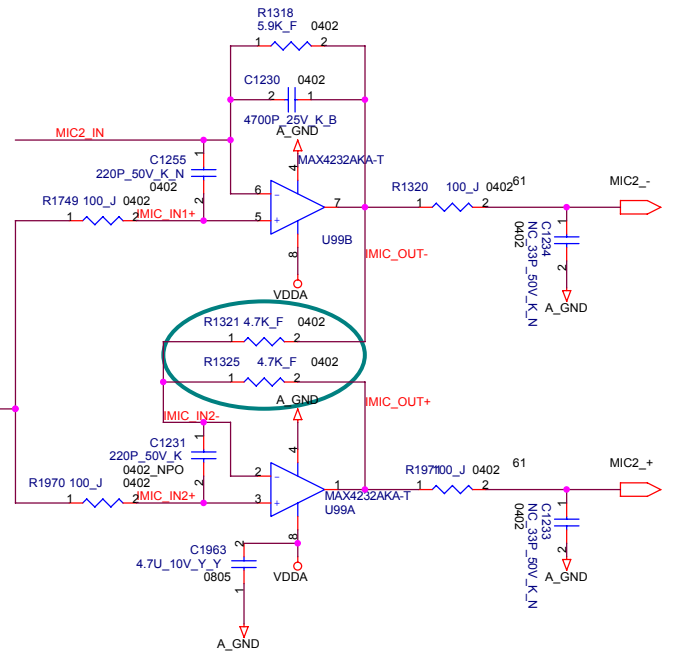


1004
Change U45, U140 as NC
For Headphone in mute speaker out
isn't supported in Dos mode
1005
Phone-out is not required

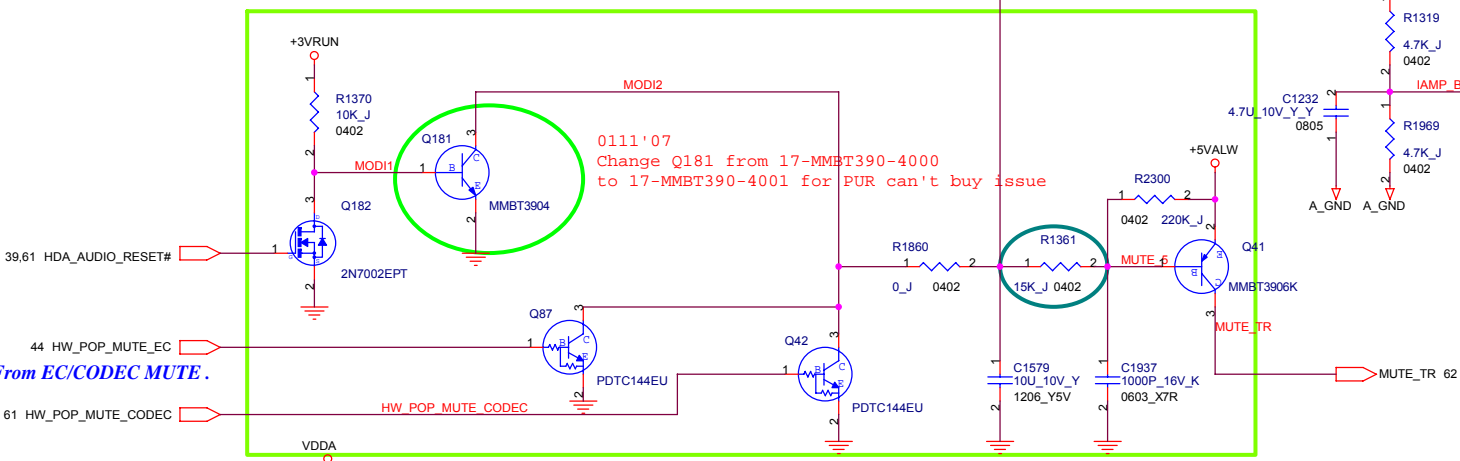
Circuit setting table

Circuit 0 (Beagle)	Circuit 1 No support Dos mute (Default)	Circuit 2 Support Dos mute	component
Stuff	NC	Stuff	U45
NC	NC	Stuff	U140
NC	Stuff	NC	R1985
Stuff	NC	NC	R1984

1025
Change Mute control circuit
(Same with MS30/50/90)



1227
Change R1321 and R1325 from 4.7k_J to 4.7K_F
for MOR Side Command.



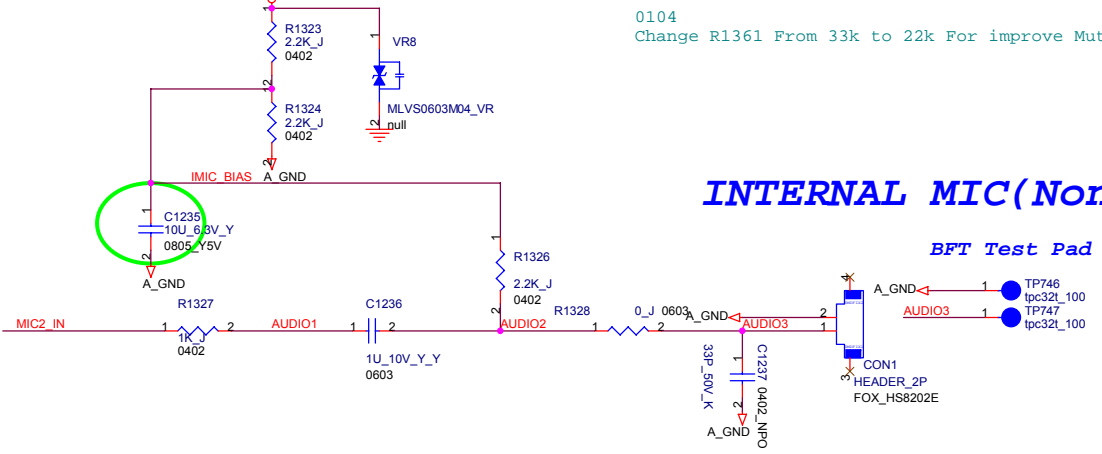
0111'07
Change Q181 from 17-MMBT390-4000
to 17-MMBT390-4001 for PUR can't buy issue

0104
Change R1361 From 33k to 22k For improve Mute_TR signal quality well.

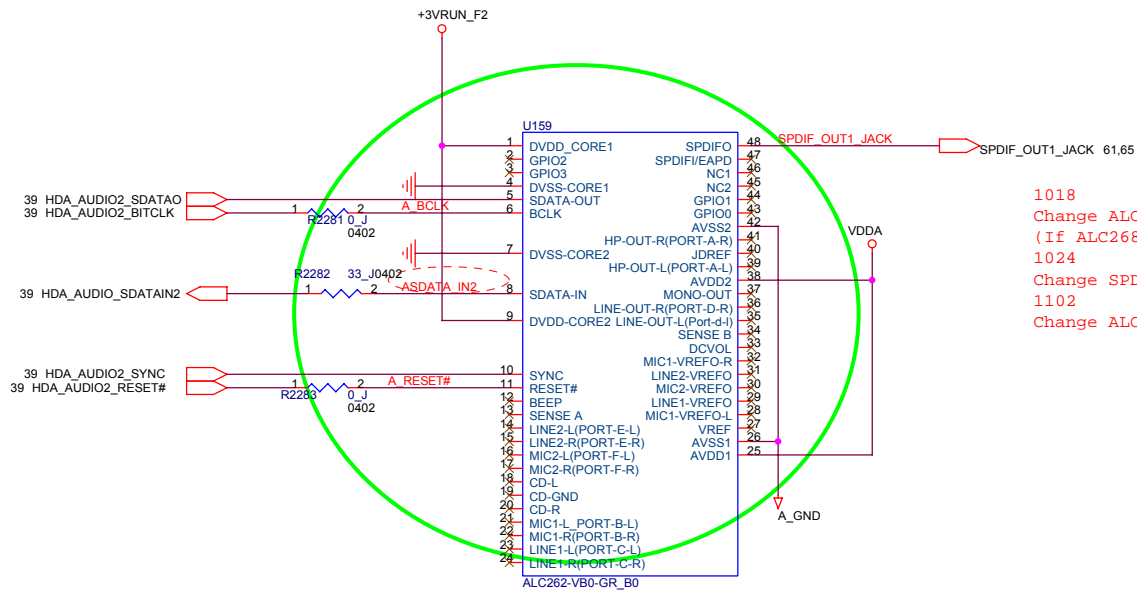
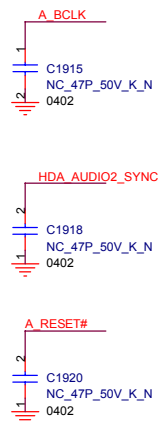
1005
Del phone-out mute circuit
for phone-out is not required

INTERNAL MIC(Non)

BFT Test Pad

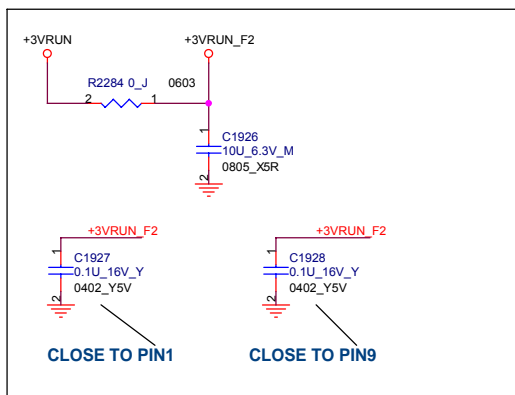


Anti-Glitch

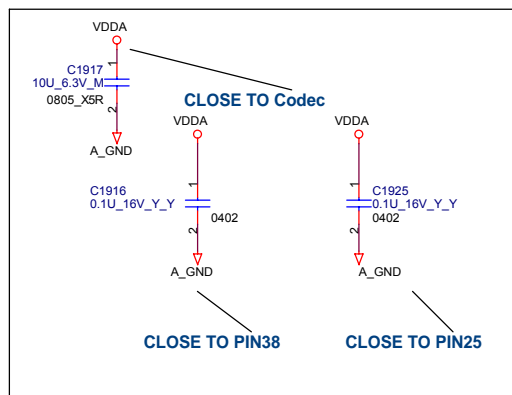


1018
Change ALC262 to ALC268.
(If ALC268 sample schdule delay, change to ALC262)
1024
Change SPDIF of Second codec to MB optical out
1102
Change ALC268 to ACL262

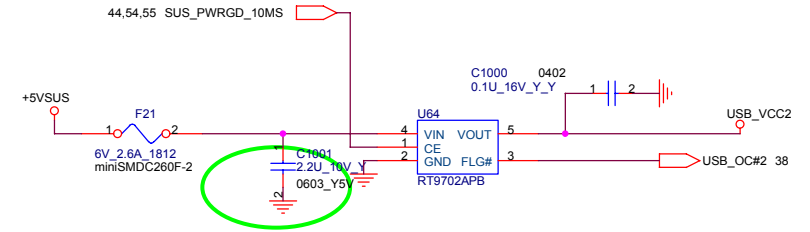
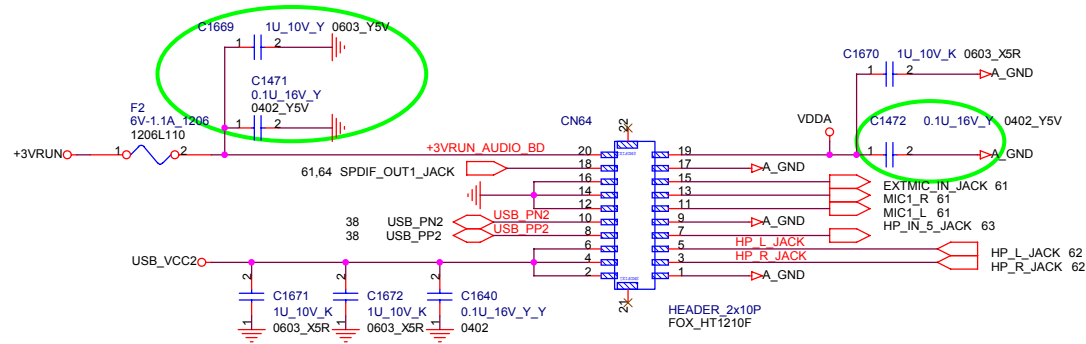
Decoupling Caps, place close to power pin.



Decoupling Caps, place close to power pin.

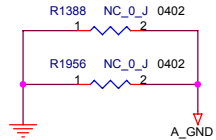


Audio Board connector

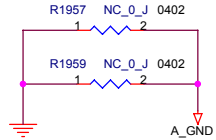


Backup two jumper resistors for bridge between GND and A_GND

Close screw hole H3

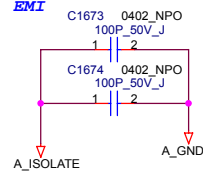


Close screw hole H5

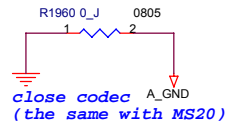
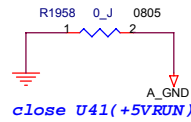
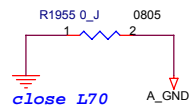


Isolate screw hole H4, and add EMI/ESD solution

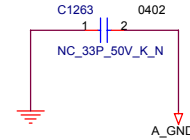
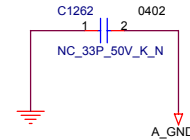
EMI



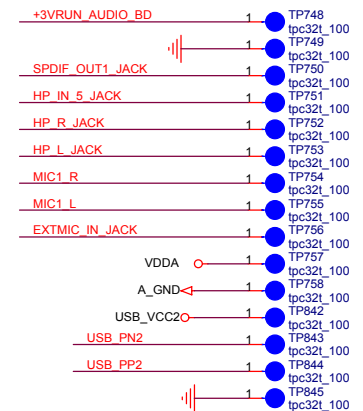
Add jumper resistor for Return patch



Original EMI back up solution to continue with MS20(bridge between GND and A_GND)



BFT Test Pad



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

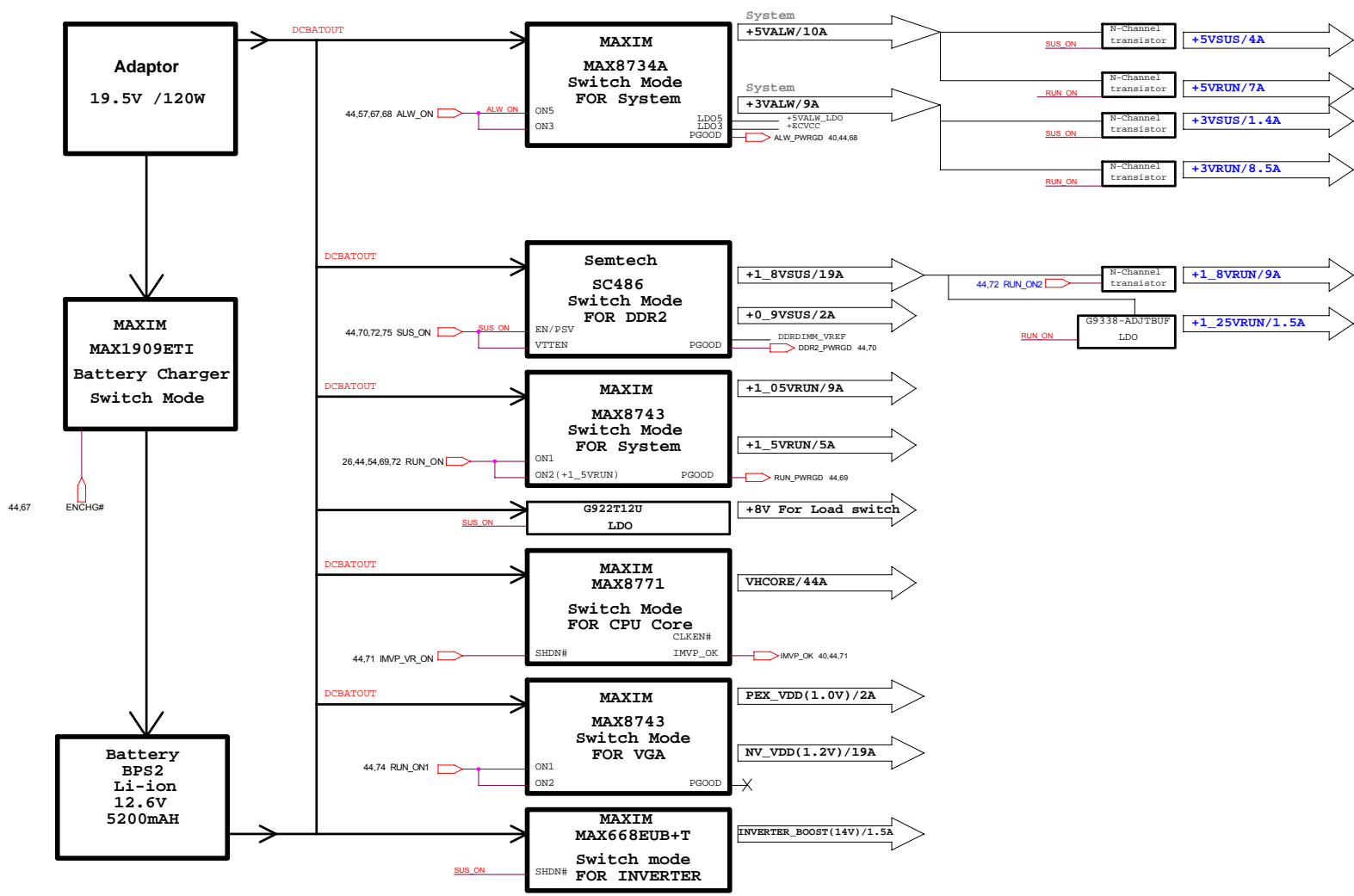
Title: Audio Board conn

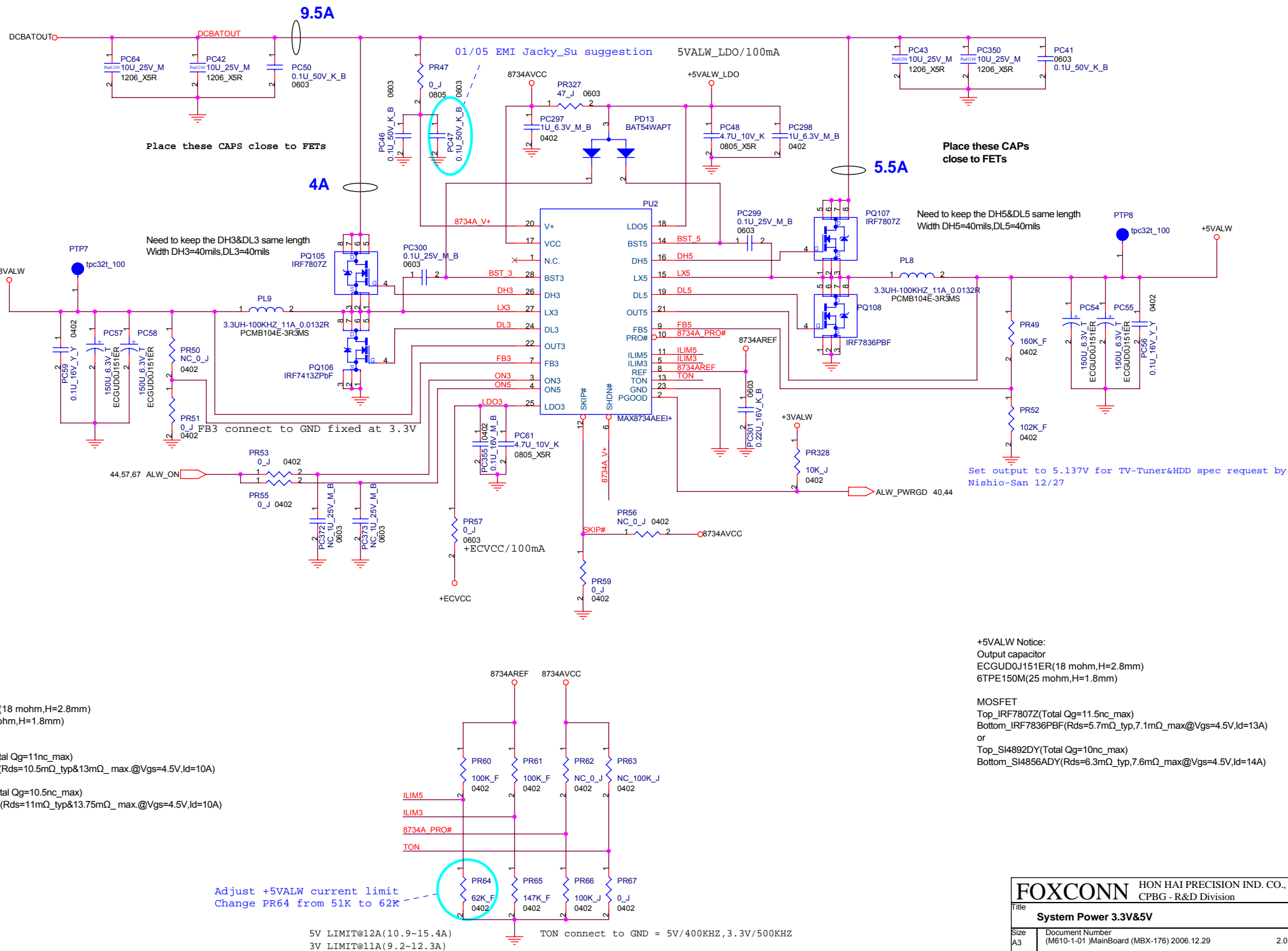
Size: Document Number

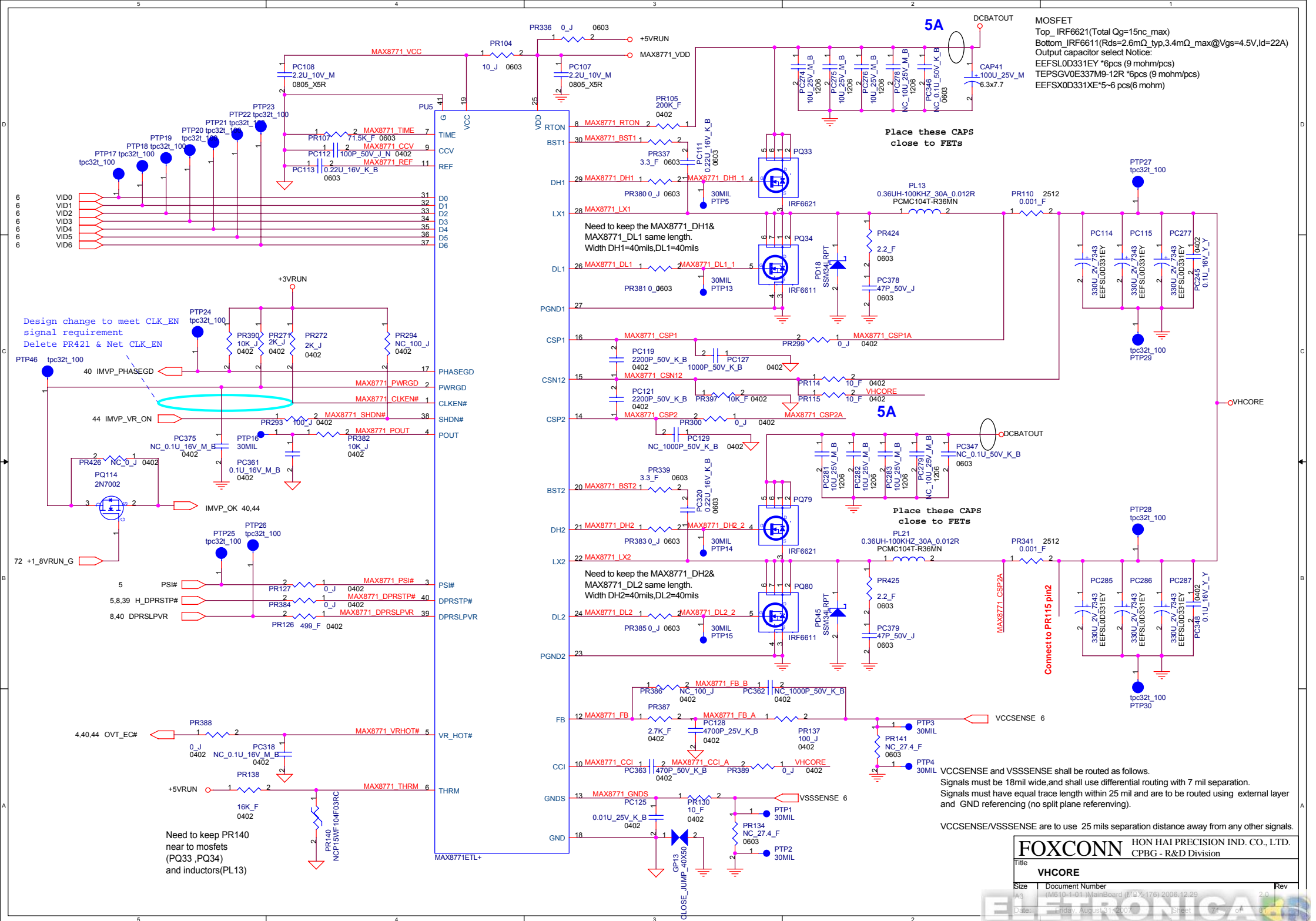
Rev: 2.0

Date: Friday, August 31, 2007

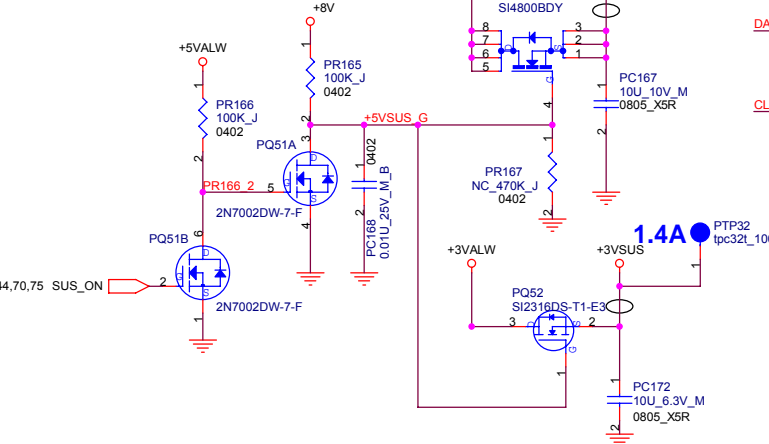
Sheet: 66 of 81



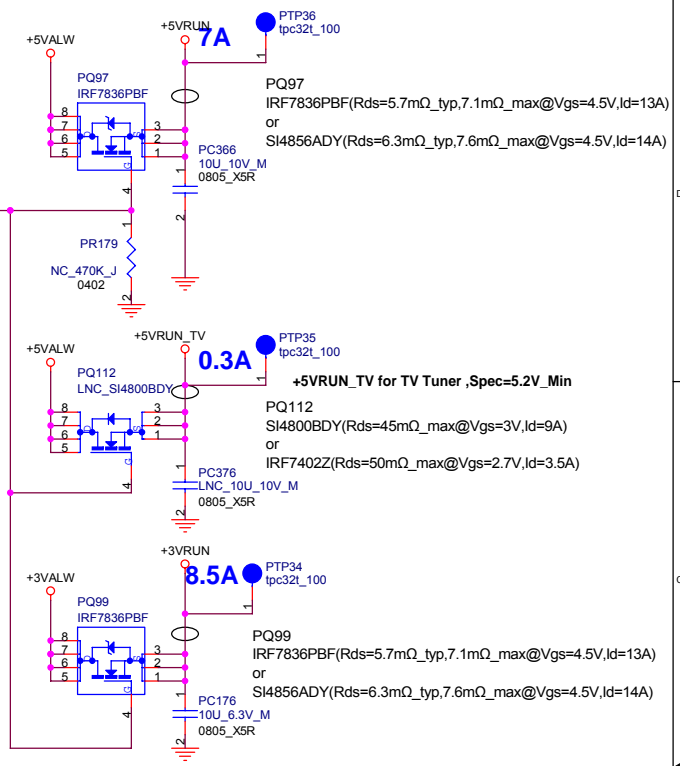
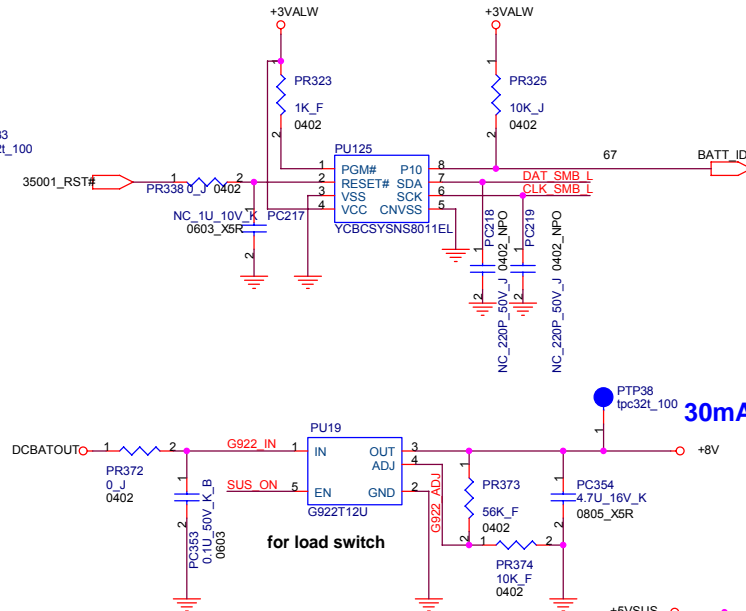
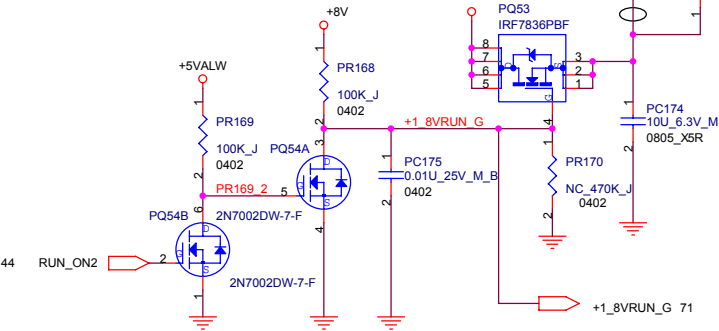




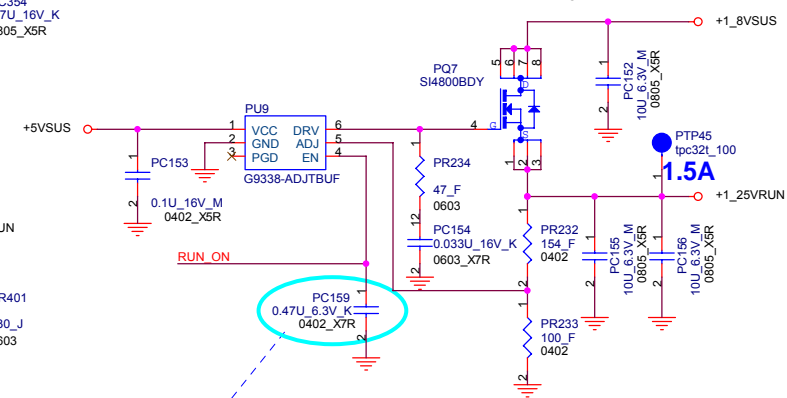
PQ50
SI4800BDY(Rds=45mΩ_max@Vgs=3V,Id=9A)
or
IRF7402Z(Rds=50mΩ_max@Vgs=2.7V,Id=3.5A)



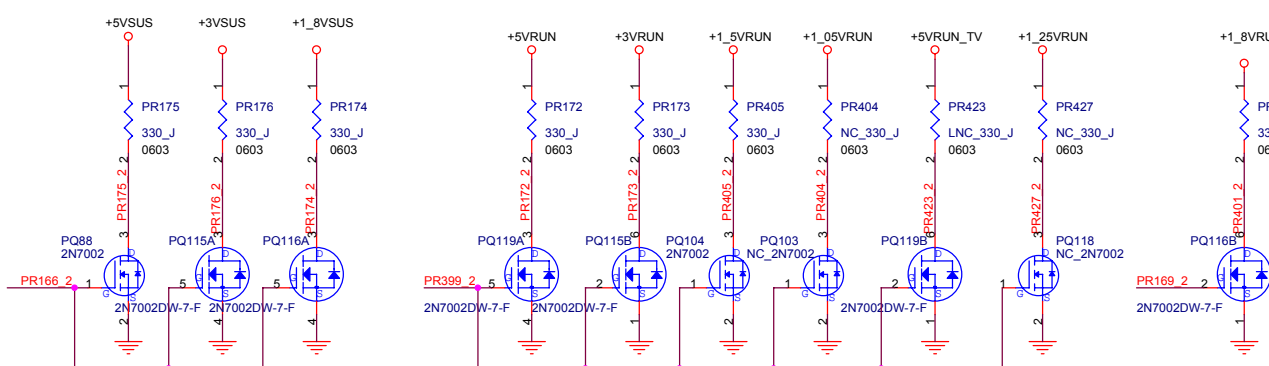
PQ53
IRF7836PBF(Rds=5.7mΩ_typ,7.1mΩ_max@Vgs=4.5V,Id=13A)
or
SI4856ADY(Rds=6.3mΩ_typ,7.6mΩ_max@Vgs=4.5V,Id=14A)



PQ7
SI4800BDY(Rds=30mΩ_max@Vgs=4.5V,Id=7A)
or
IRF7402Z(Rds=35mΩ_max@Vgs=4.5V,Id=4.1A)



Discharge circuit for power-off



11/16 PC159
shortage issue
Change X5R (1C-2B20474-M000)
to X7R (1C-2B20474-K000)

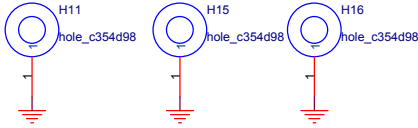
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division			
Other power plan			
Size	Document Number		Rev
A3	(M610-1-01) MainBoard (MBX-176) 2006.12.29		2.0
Date:	Friday, August 31, 2007	Sheet	72 of 81

11/16 PC391 shortage issue
Change X5R (1C-2B30224-M000)
to X7R (1C-2B30224-K000)

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title STEP_UP			
Size Custom	Document Number (M610-1-01)MainBoard (MBX-176) 2006.12.29		Rev 2.0
Date:	Friday, August 31, 2007	Sheet	75 of 81

HOLE

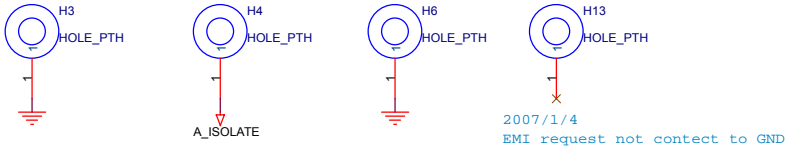
Type 1



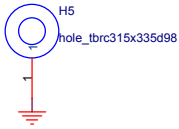
Type 2

Type 3

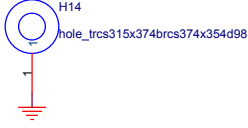
Type 4



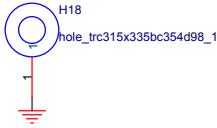
Type 5



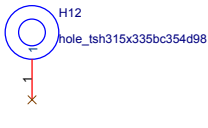
Type 6



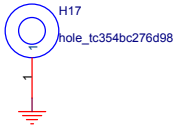
Type 7



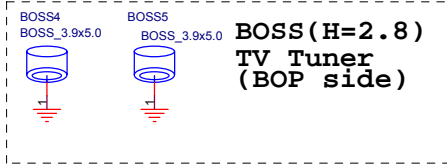
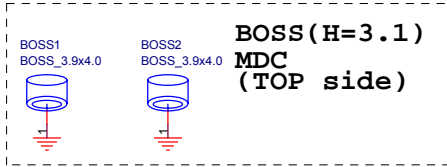
Type 8



Type 9



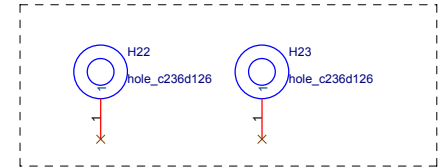
Type CPU



Type NPTH Guide (spherical)HOLD



Type NPTH Guide (oval-shaped)HOLD



VRAM Thermal Solution

M612 DVT2 Change Circuit

- 1.(Page 17~32) 07/08/17 Modify Page from 17 to 32 for 8pcs Vram.(512MB:16MBx32bx8pcs)
2. (Page 4) 07/08/29 For support Penryn-CPU, change U2-CPU Thermal Sensor from GMT to SMSC.
3. (Page 44) 07/08/29 Change System ID to M612 Type
4. (Page 76) 07/08/29 Add H22,H23 for VRAM thermal solution

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Title		CPBG - R&D Division	
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